SPAWAR

Systems Center
San Diego

TECHNICAL REPORT 1763
REVISION 2
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ADMINISTRATIVE INFORMATION

The work detailed in this report was performed for the Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA) by the Space and Naval Warfare Systems Center, Simulation and Human Technology Division, Code D44.

Released by
J. L. Martin
Deputy for Operations

Under authority of
J. D. Grossman, Head
Simulation and Human
Systems Technology
Division

PATENT STATEMENT

This technology is covered by one or more U. S. government-owned patents, patent applications and/or invention disclosures. Parties interested in licensing this technology may direct inquiries to:

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SB

EXECUTIVE SUMMARY

FIRST COMMERCIALIZED 3-D MOVING CHAMBER

First commercialized 3-D Moving Chamber. Parviz Soltan, Program Manager and Technical Coordinator, with **NEOS/RGB**-Developed 3-D System for SSC San Diego's Command Center of the Future. A single helix, 16 inches in diameter, 8 inches high, rotates at 1200 rpm with a 20-Hz image refresh rate with 256 levels of brightness. Three colors (R, G, Y) with on/off modulation. Up to 80,000 random image points per frame (1.6 million volume points per second can be drawn).

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EXECUTIVE SUMMARY

INTRODUCTION

The Space and Naval Warfare (SPAWAR) Systems Center, San Diego (SSC San Diego) Simulation and Human Technology Division has developed and improved its second-generation 3-D Volumetric Display System for displaying data, information, and scenes in a three-dimensional volume of image space. The system has good potential for many military and commercial applications. Based on a computer-controlled laser optics system that projects three laser beams simultaneously onto a 36-inch-diameter/18-inch-high double helix spinning at 600 revolutions per minute, this system presents 3-D images in an addressable 10 cubic feet of cylindrical volume.

The concept of the helix-based, laser-generated 3-D Volumetric Display was invented by Professor Rudiger Hartwig at the University of Stuttgart in Germany in the early 1980s. The concept that he demonstrated involved using a laser beam to reflect geometric figures from the surface of a rotating single helix. Dr. R. D. Williams and his team at Texas Instruments successfully demonstrated the feasibility of such a 3-D Display System in late 1989.

W. J. King and Parviz Soltan, two U.S. Navy scientists, viewed this early 3-D System Demonstration by Texas Instruments at a 1989 Technical Conference and saw the inherent military value of this promising 3-D technology. Parviz Soltan then presented a development program to the Office of Naval Research (ONR) and the Defense Advanced Research Projects Agency (DARPA) for funding. The funding was approved and the research and development began at the Laser Display Laboratory in SSC San Diego, California, by early 1990.

Since 1990, a team of scientists at SSC San Diego have recognized the dual (military and civilian) applications of a real-time, laser-generated 3-D Volumetric Display. From 1990 to 1992, the first-generation prototype of the 3-D Display System was built and tested. Later, during 1992 to 1995, an improved second-generation prototype was developed and successfully demonstrated.

The second generation was developed from four basic disciplines: laser optics, mechanics (rotating helical 3-D display), electronics (control interface), and 3-D software. The development and technical breakthroughs associated with these four areas are discussed in the first four sections of this report. The report is organized as follows:

BACKGROUND

Human visual perception relies heavily on various depth cues because the world around us is three-dimensional (3-D), yet most existing cameras and display systems can only acquire and display two-dimensional (2-D) flat images that lack the psychological and physiological depth cues of the human visual system. It is the goal of builders of the next generation of display devices to mimic 3-D depth cues as closely as possible. Examples of psychological depth cues are: distant objects appear smaller; colors of distant objects are darker; shading and shadowing of near versus distant objects, etc.

Examples of physiological depth cues are: image changes due to the motion of the observer (motion parallax), and inward rotation of the eyes when objects move closer (accommodation), etc. These fundamental restrictions of 2-D display devices greatly limit the capability of human beings in perceiving and understanding the complexity of real-world objects presented in two dimensions.

In the past 10 to 15 years, inclusion of color has become a must in both military and commercial display devices. It is expected that during the early years of the 21st century, the same will be true for 3-D display devices.

Of the leading 3-D technologies (3-D CRT, 3-D Stereoscopic, 3-D Holographic, and 3-D Volumetric), the one most compatible with the performance of the human visual system is the 3-D Volumetric Display.

3-D VOLUMETRIC DISPLAY

A 3-D Volumetric Display presents 3-D images in true 3-D space. Volume points (voxels) display real 3-D images to viewers for group viewing. This technique (see figure 1) replaces the flat screen of the 2-D display with a rotating helix. The 3-D image is projected on the surface of the helix with computer-directed laser beams. As the helix spins faster and faster, it becomes invisible; however, its reflective helical surface simultaneously receives and reflects all the laser-projected image points.

Based on the image point's 3-D coordinates (x,y,z) and the rotational speed of the helix, the computer calculates where the surface of the helix will be at any moment and directs the laser beams onto its surface. All computer-generated 3-D images are created by pre-storage in the computer or in real time. The 3-D Volumetric Display provides, like the human eye, depth cues for our visual systems, thus aiding in the perception of the 3-D objects. All the 3-D images can be viewed by multiple viewers around the device up to 360 degrees with no eyewear necessary.

WHY 3-D VOLUMETRIC DISPLAY?

What motivates the current interest in developing 3-D Volumetric Display? Because it is very close to the depth perception of the human visual system, it has become one of the leading 3-D techniques that could have dual military and commercial use. Examples include the following:

a. **Air Traffic Control** is one of the most stressful jobs today. This is because the 3-D images must be integrated by the air traffic controller from 2-D information. Specifically, third dimension (the height of the airplane) must be separately read and fused in the mind of the air traffic controller. Studies have shown much improvement in performing air traffic tasks when 3-D volumetric display is incorporated in real time, thus, adding considerable safety to our ever-increasing, crowded airports (see figures 4, 5 and 6).

b. **Submarine Navigation** is another integration of several different types of two-dimensional data used to create a mental picture of 3-D surroundings. With the requirement that submarines operate in littoral waters, awareness of the ocean bottom has increased. In the case of the Navy's new 3-D display, sonar data of the ocean bottom terrain has been incorporated and used to demonstrate the possibility of navigating a submarine in and around a varied marine environment as well as to track the movement of other objects in the water (other submarines, mines, torpedoes), and to display all this information on one 3-D display. Also, this 3-D display device may enhance viewing functions of the periscope in submarines by providing 3-D images 30 ft, or more, below the water. Present plans are to interface the display to real-time inputs in a manner similar to the air traffic control scenario described above.

TECHNICAL OBJECTIVES

First-Generation System

This system featured a 13-inch-diameter double-helix configuration. The system utilized a single laser (green) and a single acousto-optic (AO) scanner, which was later upgraded to multicolor lasers and additional scanners. This early device, while limited in capability (4000 image points or voxels per color at 20 refreshes per second), proved the technology was feasible and had potential applications to many military platforms and commercial users.

The Second-Generation System (See figures 1 and 2)

The second-generation system was significantly upgraded with multiple color, RGB (Red, Green, Blue) capability, and 40,000 image points (voxels) per color. The System also boasted a relatively noise-free 36-inch-diameter by 18-inch-high double helix that still operated at a design speed of 600 revolutions per minute and a 20-Hz refresh rate with 256 levels of brightness. Working closely with the original AO scanner contractor (NEOS Technologies Incorporated), the second-generation design increased the limit to 40,000 voxels per color (120,000 for three colors or up to 2.4 million volume points per second), which may approach the practical limits of the slow-shear TeO_2 AO random access scanners. The improved AO scanner has also been incorporated in the design and development of the first commercial model (see page 1).

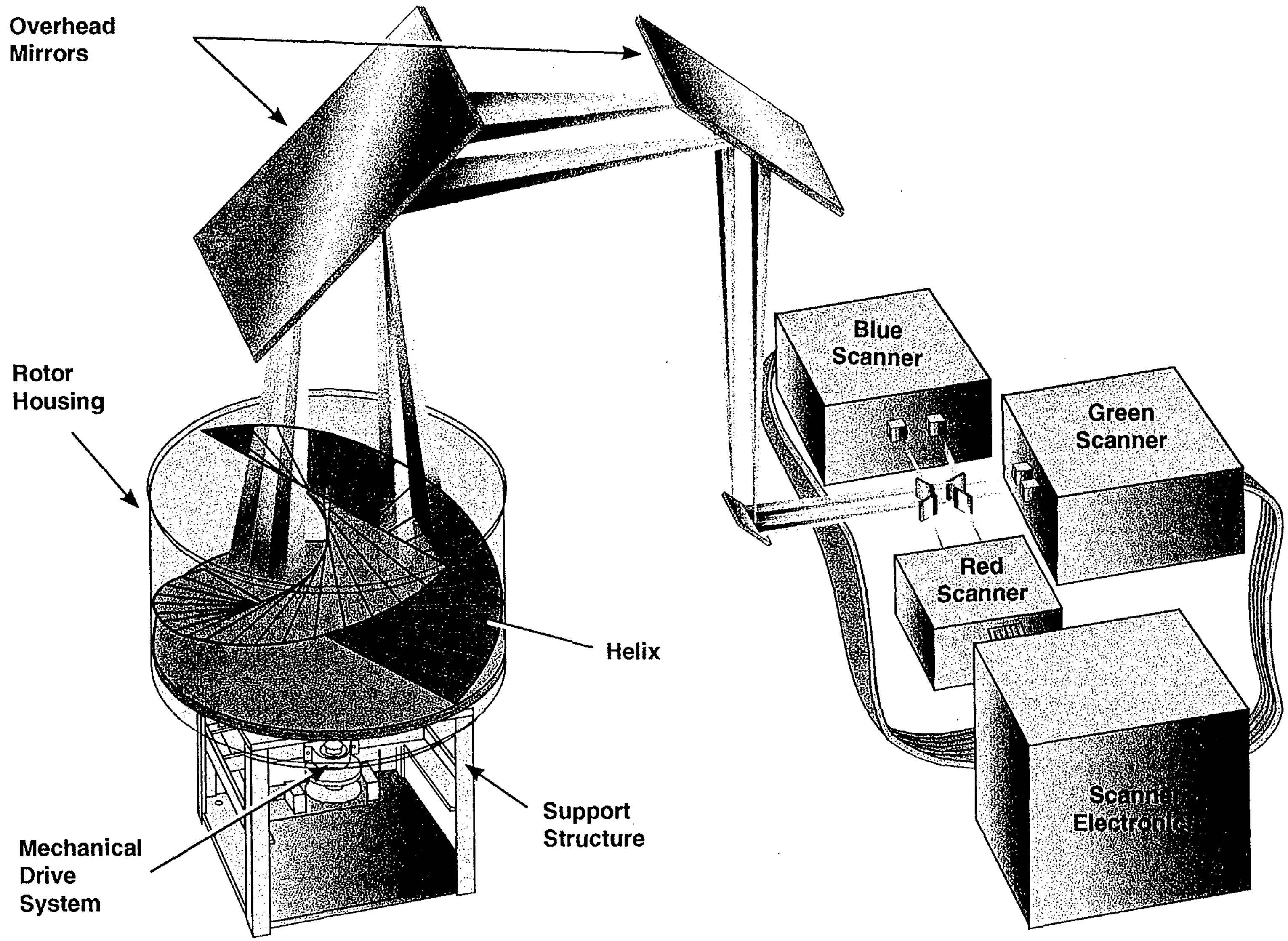

Figure 1. Second-Generation 3-D Volumetric Display System (36-inch laboratory model).

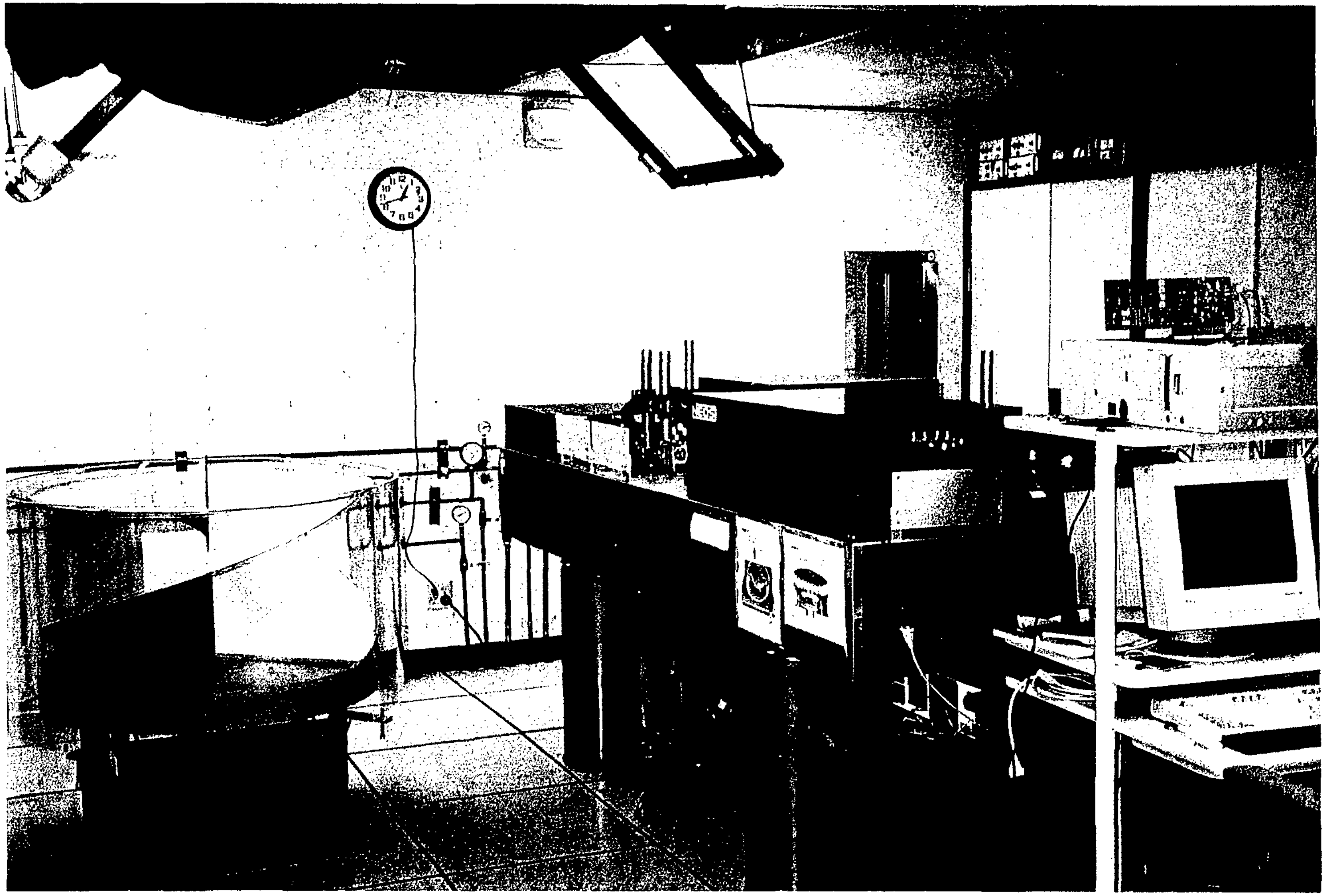

Figure 2. 3-D moving double helix at SSC San Diego Laser Display Laboratory, San Diego, CA (10 February 1998). A double helix, 36 inches in diameter, 18 inches high, rotating at 600 rpm with 20-Hz image refresh rate. Four colors (R, G, B, Y) and 256 levels of brightness. Up to 120,000 random image points per frame (2.4 million volume points per second) can be drawn.

The Transportable and First Commercial Unit (See page 1)

The Transportable

During 1995, the SSC San Diego engineering team developed the transportable 3-D Volumetric Display System for naval applications where the size of the display is a major concern. An example is the Submarine Attack Center, where a large-volume 3-D display is not desirable. To make the system as compact as possible, the helix surface material was changed to a translucent material (20 mil polystyrene), allowing laser projection to come from below the helix. Also, the helix diameter was reduced to 12 inches, allowing a much shorter projection distance for the laser scanners positioned below. The AO scanners for this system produce 10,000 voxel images at a 20-Hz refresh rate. They are similar in design to one channel of the scanners used on the larger 36-inch system. Two such scanners were used, one for red, using a 20-mW HeNe laser (633 nm), and one for green, using a 100-mW doubled-diode-pumped Nd:YAG laser (532 nm). The voxel size is 0.7 mm. The interface electronics and programming schemes were similar to those on the larger system described earlier.

Undesirable occlusion zones occur when one of the helix's double blades blocks a portion of the displayed image. Another advantage of the translucent helix is the improved viewing angle around the display created by projecting the laser beams from below. Measurements made of the occlusion zones of this system show a significant increase in viewability over the reflective larger double helix.

Commercialized Transportable 3-D Volumetric Display System (See page 1)

It became evident by the end of 1995 that commercialization of this promising 3-D technology was required for its continued growth and support. To facilitate the commercialization efforts, a Naval Cooperative Research and Development (CRADA) was signed with two American companies: NEOS Technologies of Melbourne, Florida, and RGB Technology Inc. of Reston, VA. This effort produced a portable 16-inch system that was exhibited at the International Air Traffic Controller Association Conference in Nashville, Tennessee. An upgraded model was demonstrated at the prestigious Joint Warrior Interoperability Demonstration (JWID) 1997 onboard the Navy's largest aircraft carrier, USS *Stennis*, in Norfolk, VA. In its November 1997 issue, the official Armed Forces Communications and Electronics Association Magazine, *Signal*, devoted its front cover to the NEOS/RGB-developed 3-D Volumetric Display System, calling it the "Warrior's Crystal Ball." This CRADA has reached a high point with the addressing of a four-quadrant-capable system where the entire volume occupied by the helix was accessible. The 16-inch-diameter by 8-inch-high helix rotates at 1200 rpm with a 20-Hz image refresh rate and 256 levels of brightness. It can produce three colors (R, G, Y) where up to 80,000 random image points per frame (1.6 million image points per sec) can be drawn (see page 1). The first of these commercialized 3-D systems was recently purchased by the U.S. Navy and has been installed in the newly configured and upgraded Command Center of the Future (CCOF) at SSC San Diego.

System Demonstration (See figures 3 through 7)

By the end of 1996, the Navy's second-generation 3-D Volumetric Display System had been demonstrated to many communities by newspapers, technical magazines, and TV media. Several television programs such as Discovery Channel's "Next Step" of San Francisco, "KUSI" TV from San Diego, and the British Broadcasting Corporation's (BBC) "Tomorrow World," televised the first Air Traffic Control of San Diego's Lindbergh Field recorded live and in 3-D. Also, the first-ever, live transmission of digitized 3-D images from a 3-D solid-state camera into the Navy's 3-D Display System (both at close range and via Internet) was televised by BBC to its 120 million United Kingdom viewers during November and December 1996.

3-D images presented in figures 3 through 7 are inherently true volumetric 3-D images. However, because the text is written on flat 2-D paper, the real volumetric 3-D effect is lost in the 2-D photos. In fact, no slide, photograph, painting, flat computer screen, or video is capable of displaying true 3-D.

NOTE: The 3-D images presented in this photo are inherently true volumetric 3-D images. However, because the text is written on flat 2-D paper, the real volumetric 3-D effect is lost in the 2-D photos. In fact, no slide, photograph, painting, flat computer screen, or video is capable of displaying true 3-D.

Figure 3. 3-D display of 10 a.m. air traffic at Lindbergh Field in San Diego, CA. The first line is the flight number, the second is the angular approach, the third is range in miles, and the fourth line is the height of the airplane in feet.

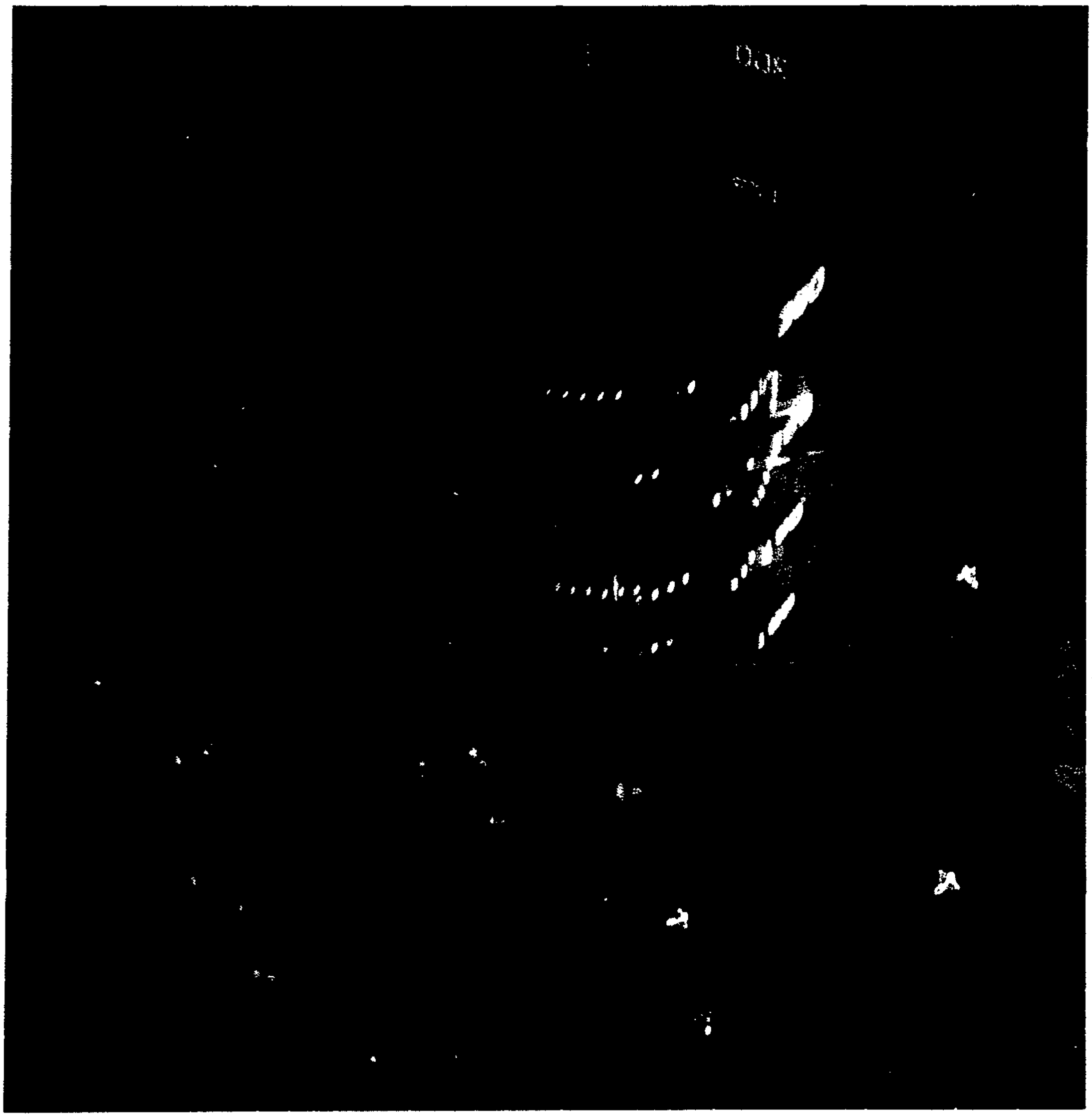

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Figure 4. Zoom technique for a limited window of air traffic. Only planes in the space window between 10,00 to 20,000 feet are monitored. The first line is the flight number, the second is the angular approach, the third is range in miles, and the fourth line is the height of the airplane in feet.

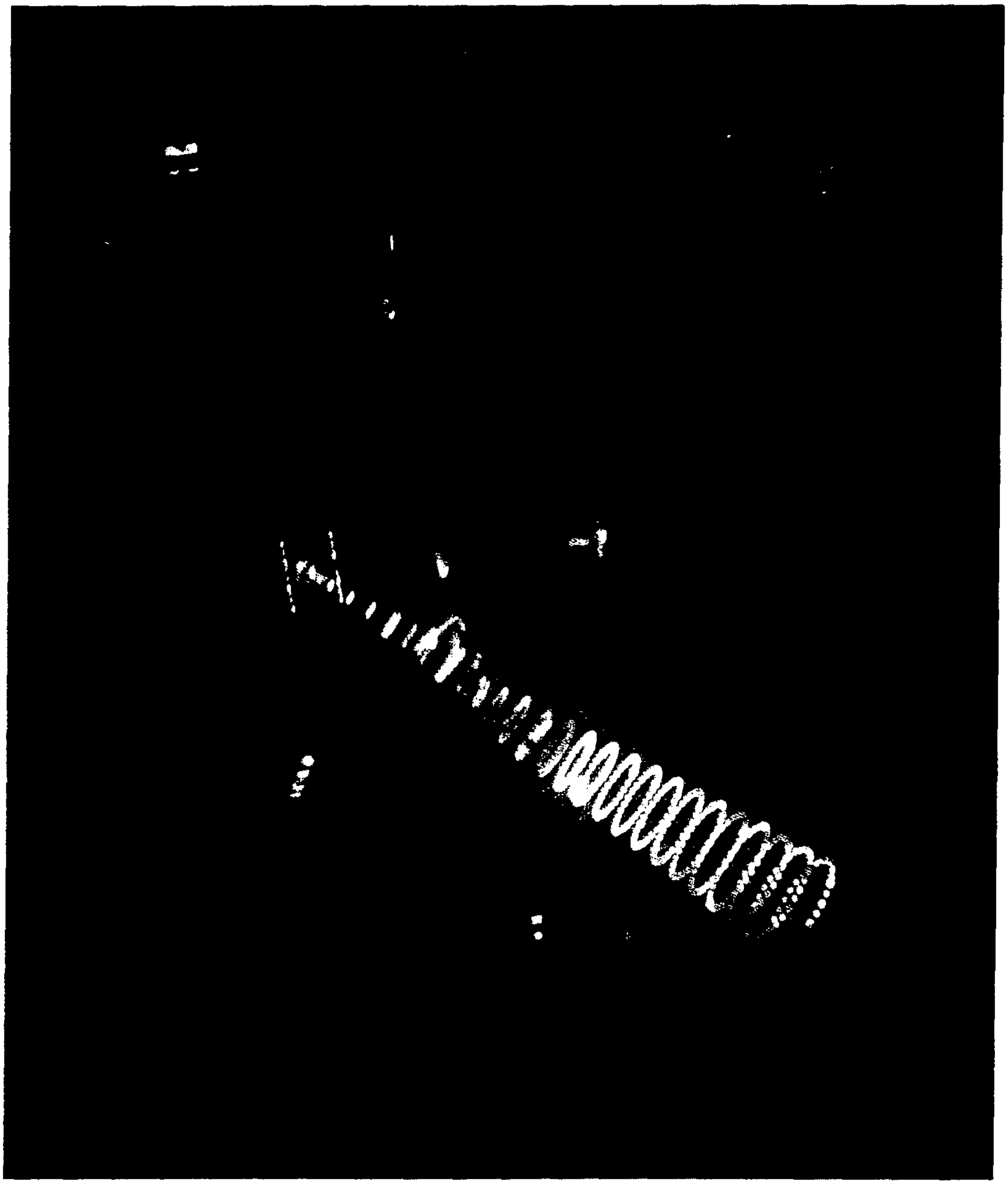

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Figure 5. Radar-generated Cone of Approach Technique for safe landing below 4,000 feet. The radar-generated cone (red) is from air traffic control to the sky. Plane permitted to land also generates a radar cone (green). At 4,000 feet, where the two cones of approach coincide (yellow cone), the landing becomes automatic and safe. The first line is the flight number, the second is the angular approach, the third is range in miles, and the fourth line is the height of the airplane in feet.

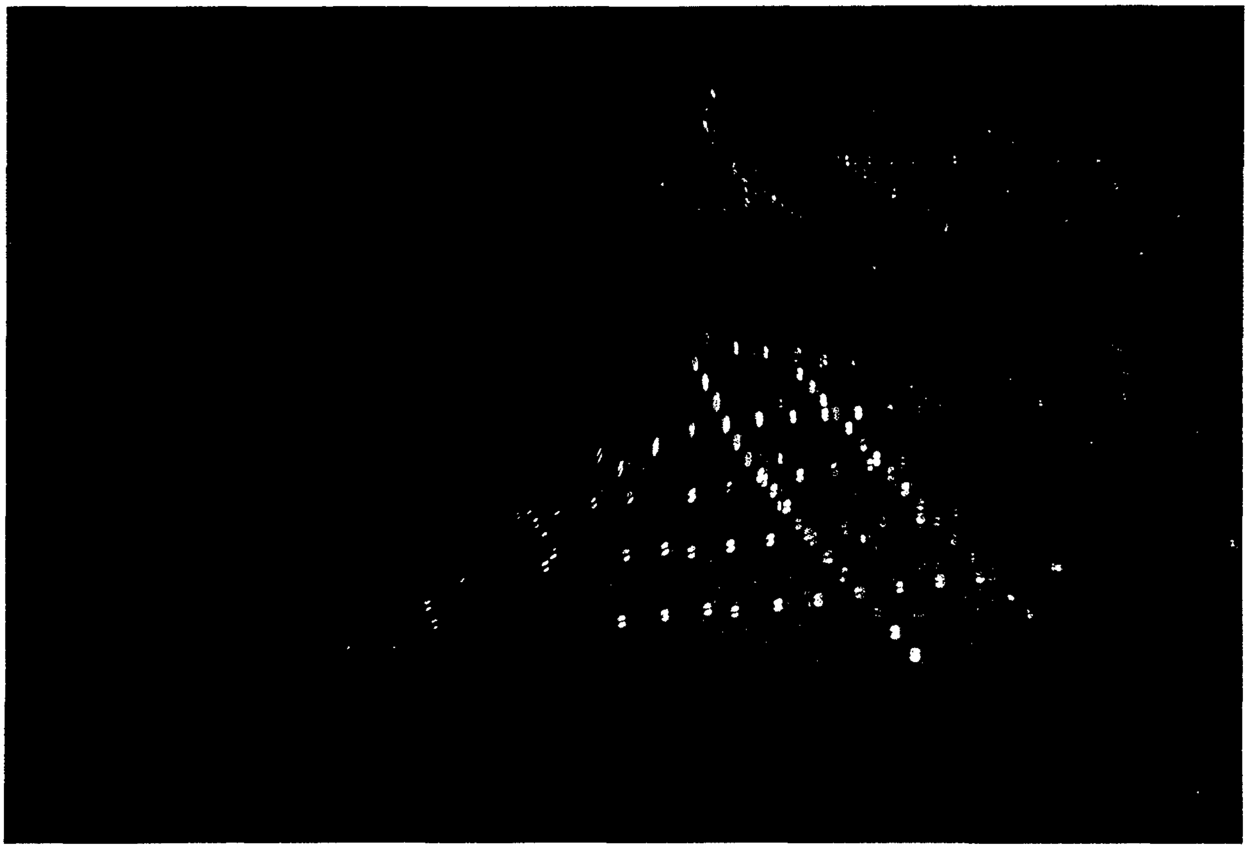

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Figure 6. 3-D Volumetric Display applied to anti-submarine warfare. This display would provide true 3-D images and color for group viewing in the Submarine Attack Center to guide the submarine in shallow waters, live and in real time.

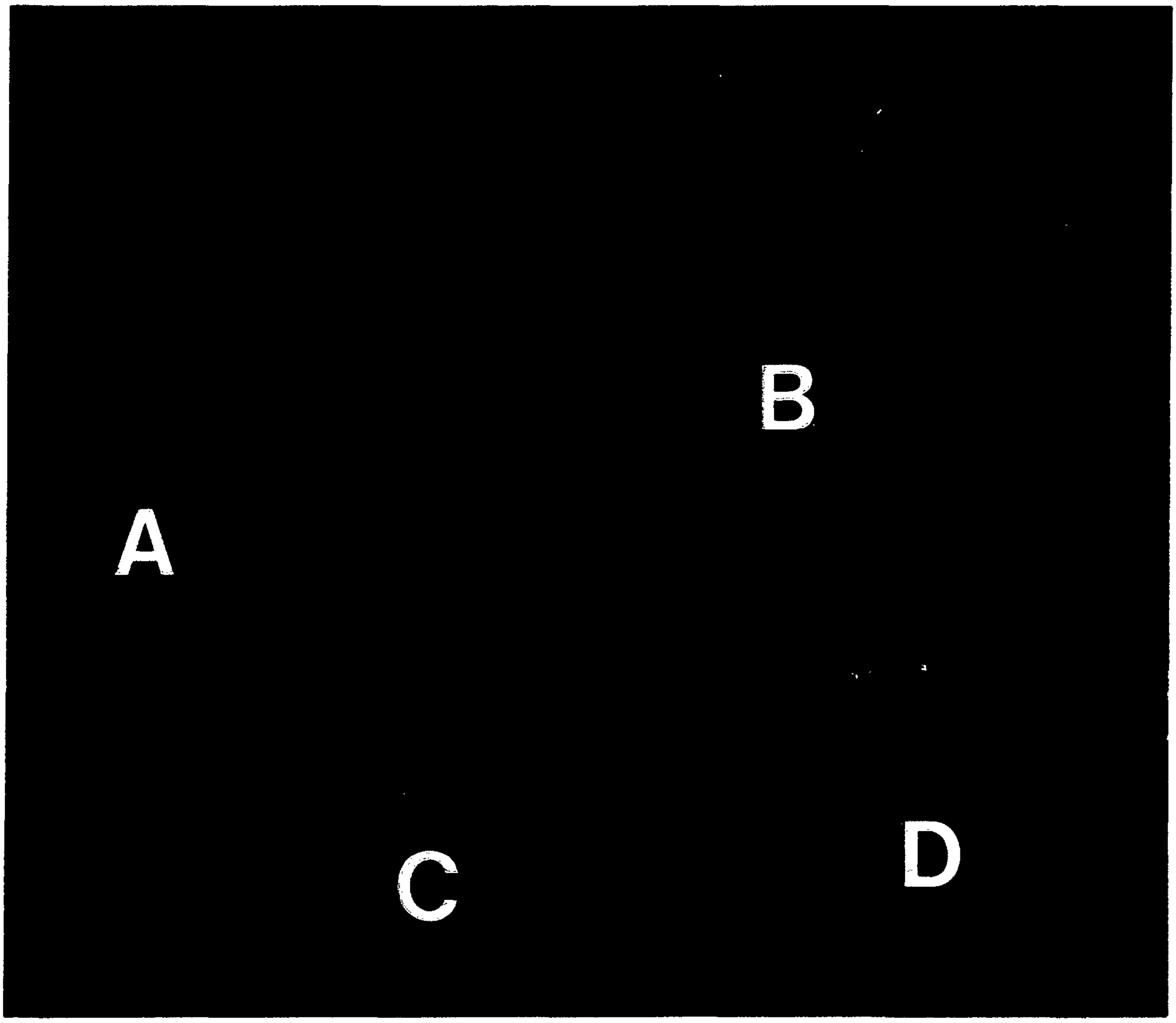

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Figure 7. Simultaneous 3-D display of four medical images: (A) arteries of a human heart; (B) molecular distribution of an aspirin in 3-D; (C) DNA molecules in 3-D; (D) electrocardiogram in 3-D. Illustration shows four images in one image frame. Only four channels of 12 available channels are used. Total image points less than 3,000.

WHAT IS NEXT? WHERE DOES THIS 3-D TECHNOLOGY GO FROM HERE?

1. Third-Generation 3-D Volumetric Display System

The first commercialized model of the 3-D Volumetric Display System, which is currently installed in the U.S. Navy's Command Center of the Future (CCOF) at SSC San Diego, was introduced in July 1997 at the JWID 97 Technology Demonstration onboard the U.S. Navy aircraft carrier, USS *Stennis* in Norfolk, VA.

The commercial system was demonstrated in the ship's Tactical Flag Command Center (TFCC), and many U.S. Navy Flag Officers and other senior officials viewed the 3-D Volumetric Display System as a critical future technology worthy of further development by the Navy. Many commented that future development efforts should increase the SIZE and RESOLUTION of the next system.

a. Proposals are currently under consideration for developing a third-generation system. This system will feature a larger 3-D display chamber based on a single translucent helix (4 feet in diameter by 2 feet high, weighing less than 100 pounds, including its housing) that will receive up to 600,000 voxels (five-time improvement) at a 20-Hz refresh rate, amounting to 12 million image points per second.

b. A new AO scanner configuration designed at SSC San Diego will provide a large increase in the 3-D image resolution (from 120,000 to 600,00 points per image frame). The configuration will be implemented in the new, improved 3-D Volumetric Display System. There are many possible military applications. For mission planning and target manipulation, the new high-resolution 3-D Volumetric Display System would utilize data from the Joint Maritime Command Information System (JMÇIS) to provide, in real time, the annotated air tracks, radar coverage zones, air corridors, collision avoidance warning, fire control zones, and helicopter landing zones. For undersea operations, the 3-D System could use data from bathymetric maps, submarine tracks, acoustic fields, temperature fields, and sound-speed profiles.

2. Technology Breakthroughs

a. Electro-optic (EO) Random Scanner

As the acousto-optic laser scanners used extensively in the 3-D Volumetric Display Systems may soon reach their image-point-generating limits, EO scanners are being investigated. EO scanners could increase the number of available voxels over a million per color, providing a much smoother and natural image. This technology began in 1994 between SSC San Diego and the University of California San Diego (UCSD). Under an ONR contract, there has been considerable progress. The future of this EO Scanner technology is very promising.

b. Improved Spatial Light Modulator/White Light Approach

The latest development in Space Light Modulation (SLM), using Ferroelectric Liquid Crystal and parallel image points processing, has created opportunities to modulate the image frames more than several thousand times per second. The use of SLM with white light projection instead of lasers and AO scanners could have a very positive impact on the performance and cost reduction of the Navy's 3-D Volumetric Display System.

It should be remembered, however, that the increase in the total image points should not sacrifice the image sharpness, contrast ratio, and the brightness. The preliminary reports and

observations point to these important deficiencies that must be rectified before any consideration.

c. Solid-State Non-Moving 3-D Chamber (Future 3-D Color TV)

Another important breakthrough technology is the solid-state, non-moving 3-D chamber with an infrared laser system for 3-D imaging. Development of this technology began in 1992 under an ONR contract between SSC San Diego and Stanford University. It has recently led to a commercialization effort by a small Stanford University spin-off company in Mountain View, CA. This 3-D system, under computer control, uses infrared lasers to address points within a rare-earth-infused solid glass cube. Already, simple animated computer-generated images have been produced.

This 3-D solid-state non-moving chamber coupled with the high-speed EO random laser scanner, described earlier, can provide the foundation for future 3-D color TV in the 21st century.

OTHER MILITARY AND COMMERCIAL APPLICATIONS (FIGURES 8 THROUGH 13)

Air Traffic Control (See figure 8)

For the first time, the 3-D air traffic monitoring, in real time, has been developed and demonstrated at SSC San Diego's Laser Display Latoratory with authentic data obtained from the Navy's Identification Friend or Foe (IFF) antenna. This naval 3-D Display System would provide true 3-D data in color for group viewing of air traffic. It is a safe choice for collision avoidance and the managment of air traffic in a volume of aerospace, for the FAA, the Air Force, and onboard the Navy's aircraft carriers.

Submarine Navigation (See figure 9)

This display would provide true 3-D images and color for group viewing in the Submarine Attack Center to guide the submarine in shallow waters, live and in real time. In the case of the 3-D Volumetric Display, sonar data of the ocean bottom terrain has been incorporated and used to demonstrate the possibility of navigating a submarine in and around a varied marine environment as well as track the movement of other objects in the water (other submarines, mines, torpedoes), and to display all this information on one 3-D display. Also, this 3-D display device may enhance viewing functions of the periscope in submarines by providing 3-D images 30 ft, or more, below the water. Present plans are to interface the display to real-time inputs in a manner similar to the air traffic control scenario described above.

Battle Management at Command Centers (See figure 10)

At command centers, this 3-D system would monitor real or simulated signals from networks and provide a real-time 3-D display large enough for more than 20 simultaneous viewers. It would be controlled with a spaceball-type mechanism, or hand-held lasers for target manipulation. This 3-D system would revolutionize the way strategic and tactical decision-makers view the battle in progress. In essence, it would give them the look and feel that they are truly on the battlefield. The perspective gained will contribute to more rapid and accurate decision-making. A 3-D volumetric display of the battle areas will greatly enhance command decision-making. Also, Global Surveillance and Communications is a good possibility. This is a capability that can focus on a trouble spot and be responsive to the needs of the commander.

Medical Imaging (See figure 11)

This display would provide true 3-D color images for group viewing of all the soft tissues of the body. These tissues include such major organs as the heart, lungs, and liver. This non-intrusive technology allows 3-D viewing of an unborn baby in the birth canal, live and in real time.

Command and Control Centers (See figure 12)

This 3-D display would provide tactical data collected for command review where it can be translated and displayed live in 3-D images. The perspective gained will contribute to more rapid and accurate decision-making. A 3-D display of the battle areas will greatly enhance command decision-making. Also, Global Surveillance and Communications is a good possibility. This is a capability that can focus on a trouble spot and be responsive to the needs of the Commander.

Entertainment (See figure 13)

The entertainment center of the future may include a non-moving solid-state chamber for 3-D color TV.

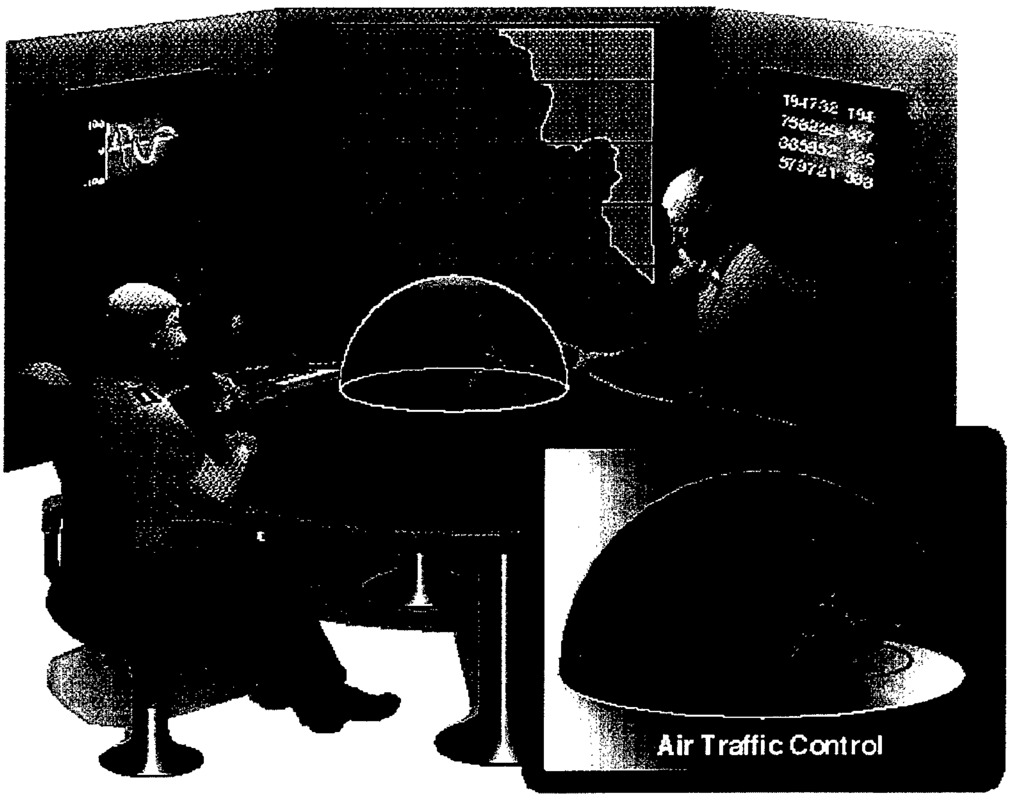


Figure 8. Air Traffic Control in 3-D. For the first time, the 3-D air traffic monitoring, in real time, has been developed and demonstrated at SSC San Diego's Laser Display Latoratory with authentic data obtained from the Navy's Identification Friend or Foe (IFF) antenna. This naval 3-D Display System would provide true 3-D data in color for group viewing of air traffic. It is a safe choice for collision avoidance and the managment of air traffic in a volume of aerospace, for the FAA, the Air Force, and onboard the Navy's aircraft carriers.

Figure 9. Live navigation of submarines in shallow waters. This display would provide true 3-D images and color for group viewing in the Submarine Attack Center to guide the submarine in shallow waters, live and in real time. Also, this 3-D display device may enhance viewing functions of the periscope in submarines by providing 3-D images 30 ft, or more, below the water.

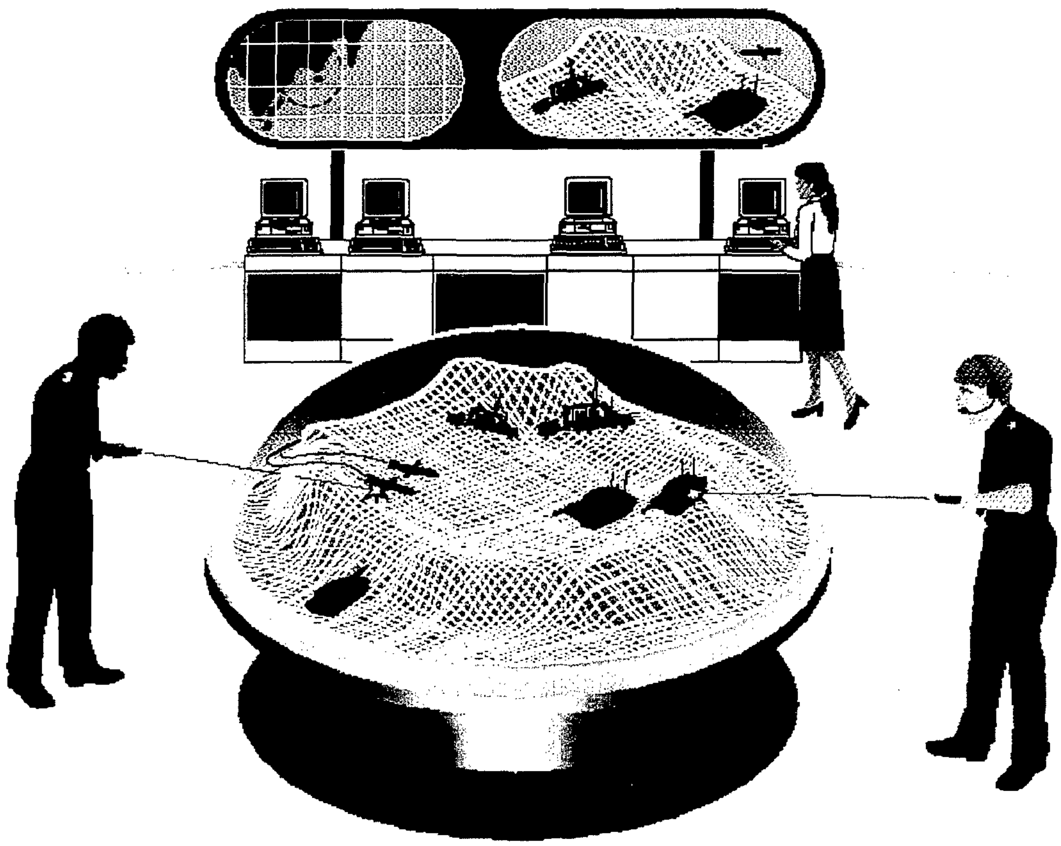


Figure 10. Battle Management at Command Centers. A 3-D volumetric display of the battle areas will greatly enhance command decision-making. This 3-D system would revolutionize the way strategic and tactical decision-makers view the battle in progress. In essence, it would give them the look and feel that they are truly on the battlefield. The perspective gained will contribute to more rapid and accurate decision-making.

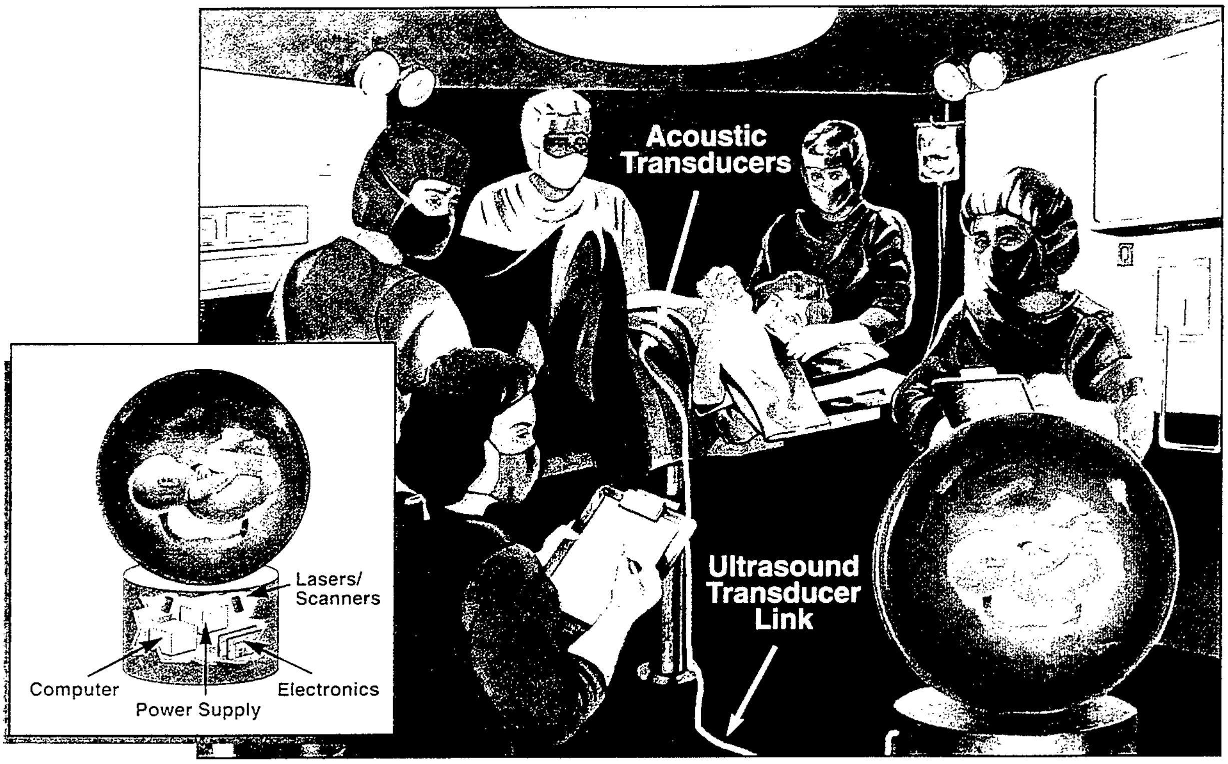


Figure 11. Future hospital operating room. This display would provide true 3-D color images for group viewing of all the soft tissues of the body. These tissues include such major organs as the heart, lungs, and liver. This non-intrusive technology even allows 3-D viewing of an unborn baby in the birth canal, live and in real time.

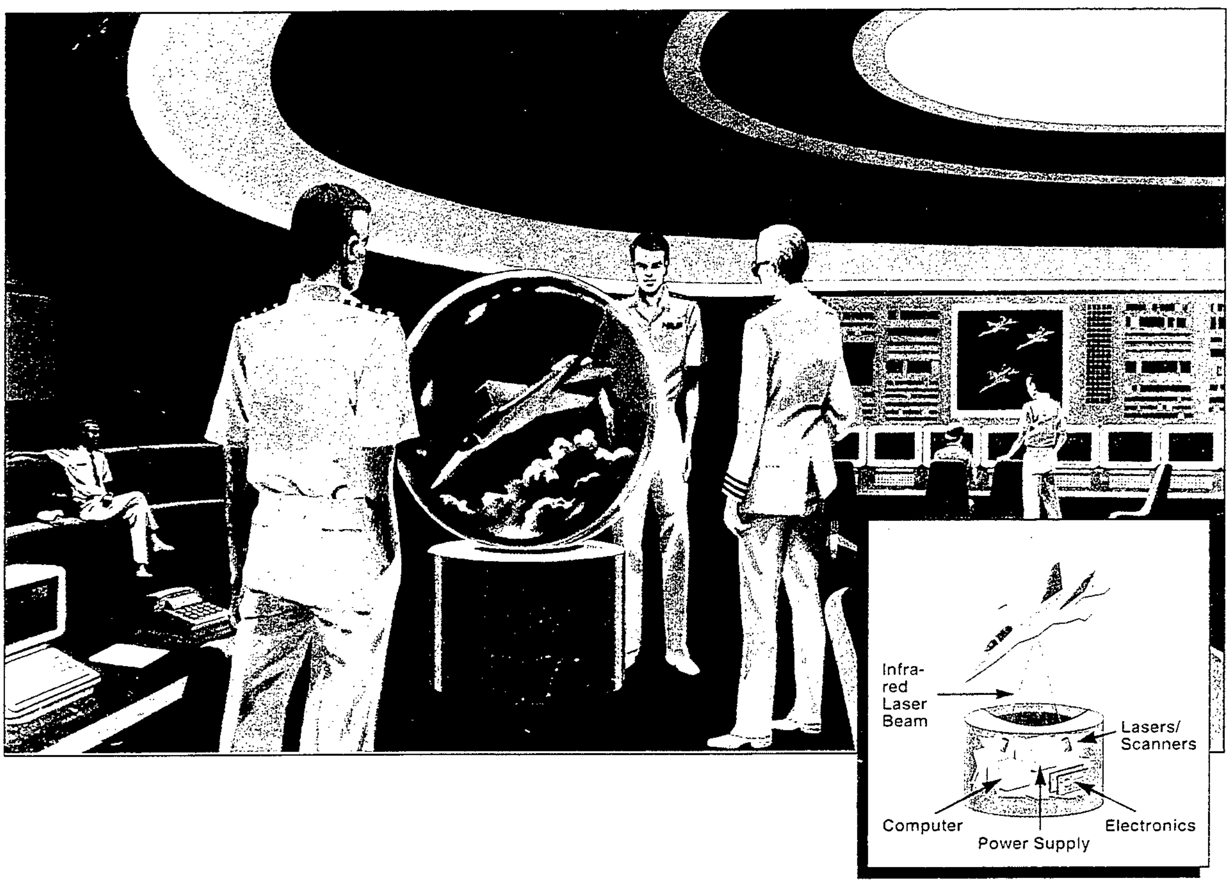


Figure 12. Future Non-Moving 3-D Display for Command Center. This display would provide tactical data collected for command review where it can be translated and displayed live in 3-D images. The perspective gained will contribute to more rapid and accurate decision-making. A 3-D display of the battle areas will greatly enhance command decision-making. Also, Global Surveillance and Communications is a good possibility. This is a capability that can focus on a trouble spot and be responsive to the needs of the Commander.

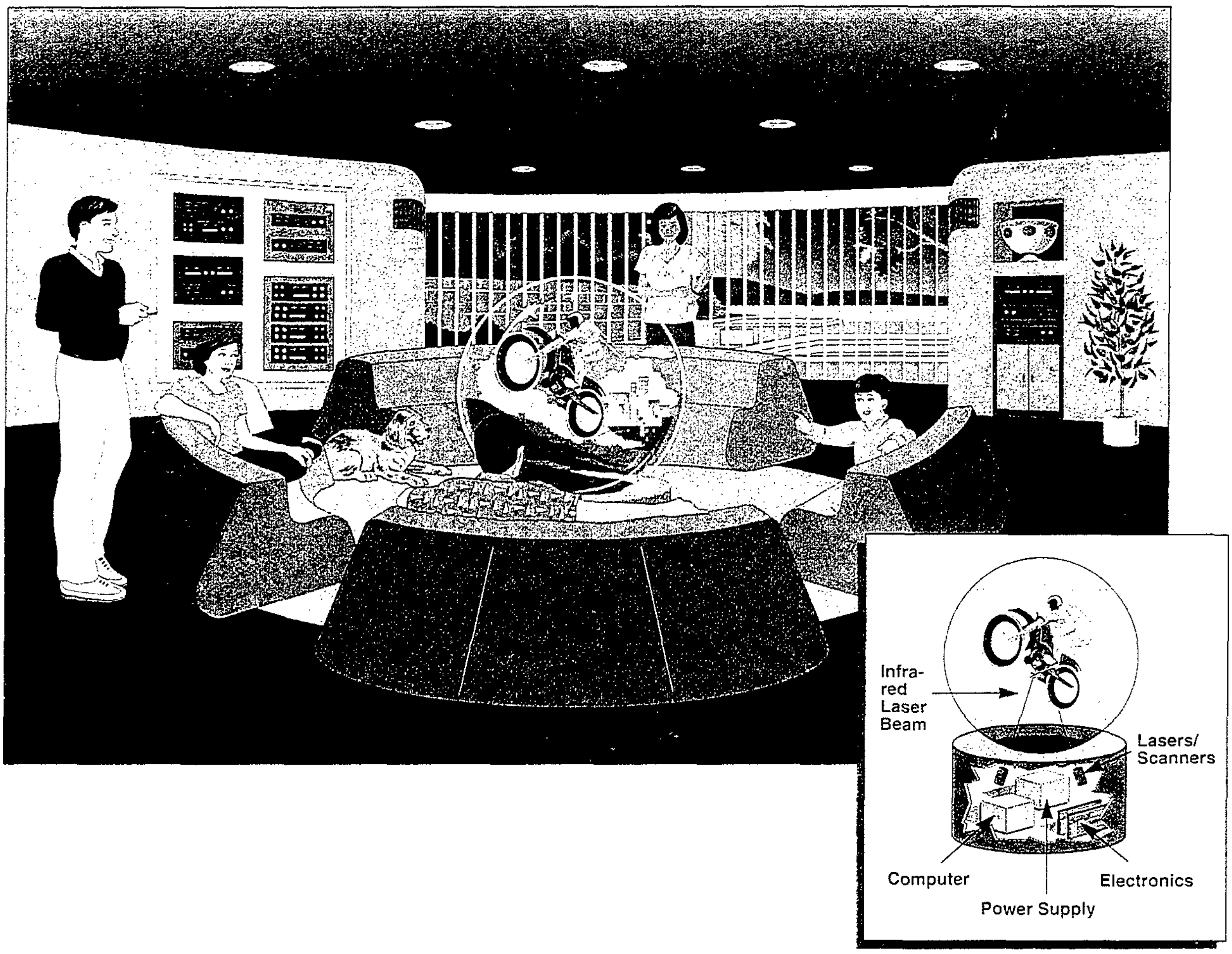
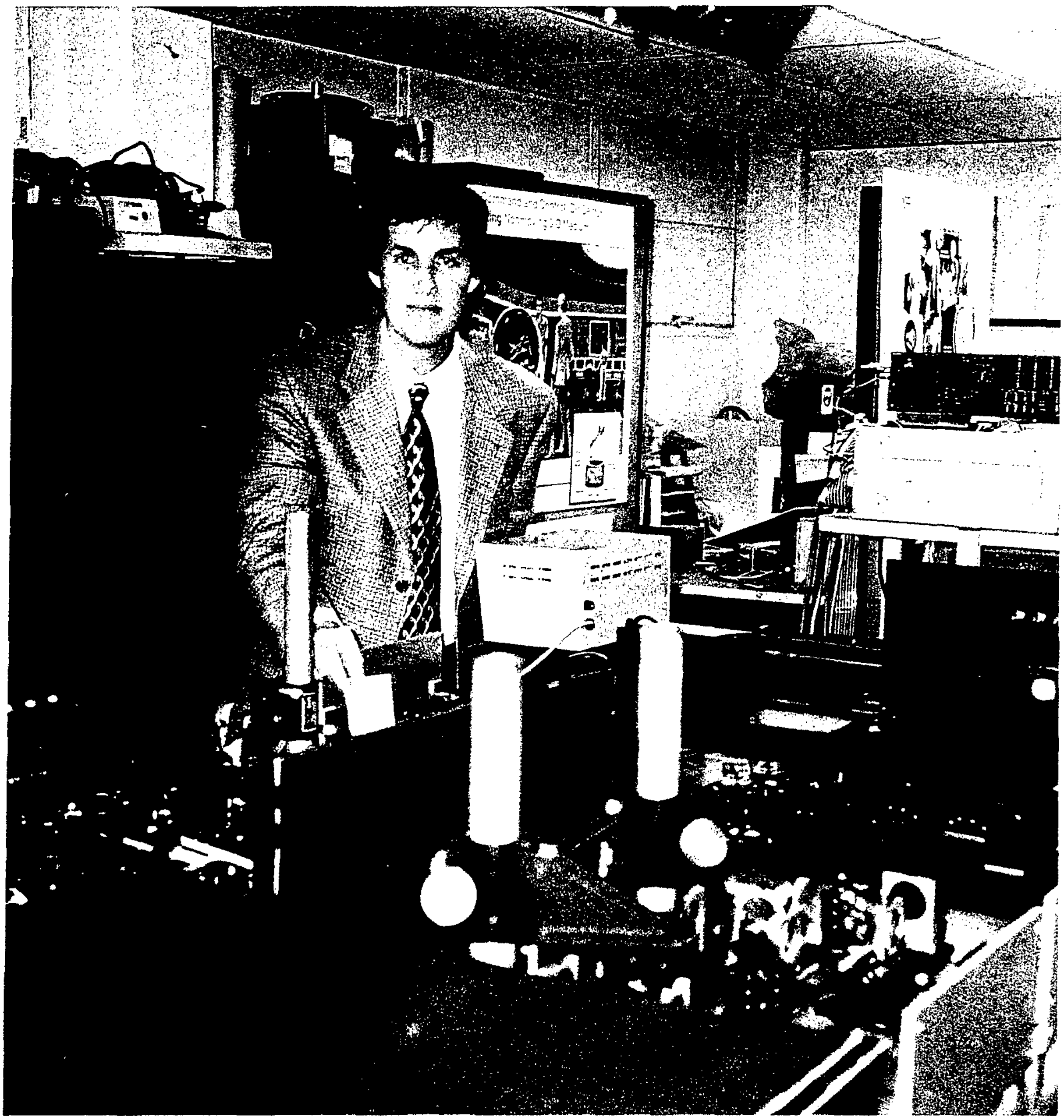


Figure 13. The family entertainment center of the future may include a non-moving solid-state chamber for 3-D color TV.

SECTION 1. 3-D OPTICS



Mark Lasher, 3-D System Optical Design Lead Engineer.

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ABSTRACT

The helix-based 3-D Volumetric Display System permits images to be displayed in a three-dimensional format that can be observed without the use of special glasses. Its rotating helical screen sweeps through a cylindrical envelope, providing a volumetric display medium through which scanned laser pulses are projected. The display images are created by synchronizing the interaction of the laser pulses and the moving screen to address a full three-dimensional volume that gives the viewer true depth cues (binocular, parallax, accommodation, and convergence) without the need for any special viewing aids. This report describes work performed over the past 5 years (1992 through 1997) on the development of the optical design for a display system based on a 36-inch diameter helix using a high-speed, multichannel, random access laser scanner. The system is capable of displaying 800,000 voxels per second. In addition, the design and construction of a transportable volumetric display and eventual transition to industry into a commercial product are detailed.

SECTION 1. 3-D OPTICS

1. INTRODUCTION

The Space and Naval Warfare (SPAWAR) Systems Center, San Diego (SSC San Diego) has an ongoing effort to display tactical data, information, and topography in a useful, interactive three-dimensional format that will enable faster and more reliable interpretation of scenes that are inherently three-dimensional. Applications include surveillance, battle management, navigation, weather systems, and air traffic control.

This section encompasses the most recent progress toward the development of a three-dimensional volumetric display using a laser-based imaging system. Previous work centered on a 13-inch-diameter double helix constructed out of a solid piece of aluminum. Two single-channel acousto-optic random access laser scanners were synchronized to the rotating helix using customized interface electronics and software. Each scanner displayed 4096 voxels at a 20-Hz refresh rate and projected red and green images onto each half of the helix. Both red and green images were obtained using a krypton-argon laser, or a diode-pumped, frequency-doubled Nd:YAG laser for the green and a helium-neon, or diode laser, for the red.

Two major requirements emerging from that work were the desire for a larger display volume and the production of more voxels in the displayed image. What follows is the design methodology used to achieve these goals in FY 93. The main emphasis here is on the optical system. Details of the helix construction, electronics, and software can be found in the other sections of this report.

2. RANDOM VS. RASTER SCANNING ON A ROTATING HELIX

One of the first questions that must be addressed in any laser scanning system is whether to use a random or raster scan approach. The simplest answer to this question can be found by considering the following. In the case of volumetric scanning, a typical volume with a resolution of 1000 voxels on each side would contain $(1000)^3$, or 1 billion addressable voxels! No scanner imaginable could update this number of voxels at a 20-Hz refresh rate. A state-of-the-art, high-speed X-Y acousto-optic raster scanner is capable of updating a 1000 x 1000 2-D image at 20 Hz. Thus, we fall only 3 orders of magnitude short of the 3-D requirement! However, the majority of volumetric images displayed on a rotating helix require illuminating only a fraction of the total addressable voxel space. Indeed, one cannot illuminate too many voxels for fear of cluttering the image, as there is no hidden line removal capability in this type of display. Raster scanning is an extremely inefficient way of trying to solve this problem as one is forced to spend most of the time scanning the laser beam to locations where no illumination is desired. The requirement of a sparse image imbedded in a dense address space makes a random scan approach a far more practical choice. With this in mind, let us look at a more rigorous explanation of the situation for a spinning helix.

First, we need some background calculations on the helix. The required rotation rate of a double helix (2 blades) designed to give a 20-Hz refresh rate is given as

$$\frac{\text{Refresh Rate}}{\text{No. of Blades}} = \frac{20Hz}{2} = 10\frac{\text{rev}}{\text{sec}} = 600\,\text{rpm}\,. \tag{1}$$

What is the speed in the z-direction of a point on the surface of the helix? The equation for the z-position as a function of the angle of rotation is given by

$$z = h\left(1 - \frac{\theta}{\pi}\right), \tag{2}$$

where h is the height of the helix and θ is the angle of rotation in radians (see figure 1-1). The velocity is then,

$$v_s = \frac{dz}{dt} = \frac{dz}{d\theta}\frac{d\theta}{dt} = -\frac{h}{\pi}2\pi f = -2\,hf, \tag{3}$$

where f is the rotation rate of the helix. For a helix rotating at 10 rev/sec and having a height of 18 inches (457.2 mm), the vertical velocity is 9,144 mm/sec. For a voxel on time of 1 msec, we get a vertical displacement of 9 microns. Thus, the voxels are actually thin disks instead of spheres.

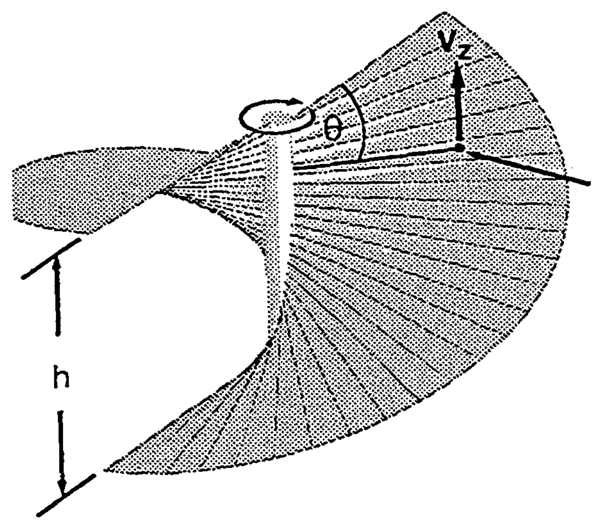


Figure 1-1. Vertical velocity of the helix.

Now consider a 1000 x 1000 raster scanner that scans a line in 50 μsec. At a 10-Hz rotation rate, one 2-D image "plane" is put on each half of the helix every 50 ms. The "plane" is actually a map of the surface of the helix, but this will be ignored here for simplicity (figure 1-2).

To simplify the discussion further, the effect of helix rotation on the manner in which the image is drawn is not strictly taken into account (such as having to start an image on one half of the helix and finish on the other). This only makes matters worse for both raster and random scanning. The discussion here is an idealized situation, the best one could ever hope for.

Returning to the 1000 x 1000 raster example, to draw 1000 planes in the z-direction would require 500 rotations of the helix! That means a complete update once every 50 seconds, obviously an unacceptable situation. One can only draw a few planes at most before flicker becomes a problem. The thought of using long-lived phosphors on the surface of the helix is dismissed on the grounds that it would only lead to a smearing of the image. Thus, we see that raster scanning is an impractical approach to 3-D volumetric helix displays.

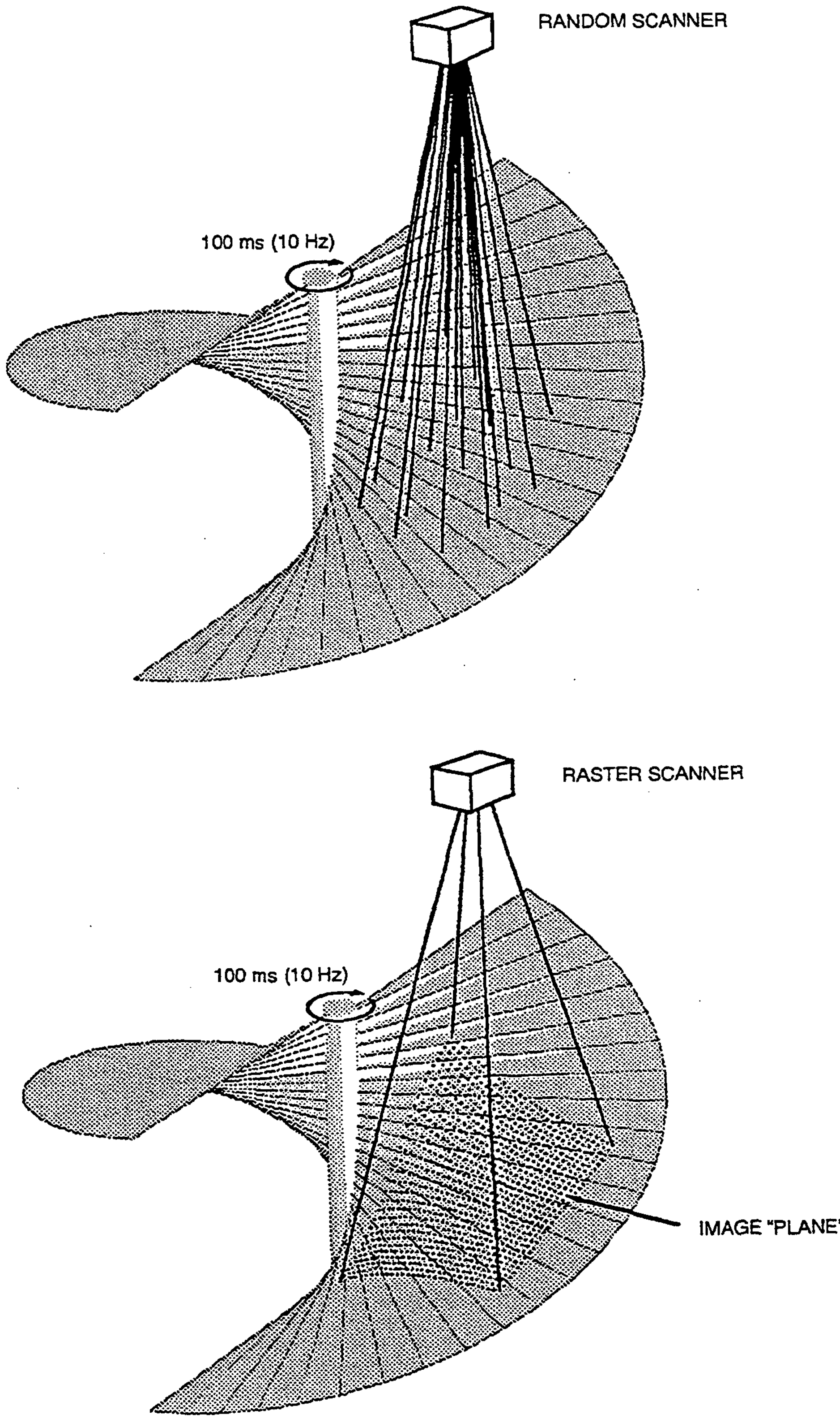


Figure 1-2. Random vs. raster scanning on a helix.

A random-access scanner provides a more efficient means of projecting an image into a volumetric display. Through proper electronic synchronization, only those voxels that comprise the image are illuminated, while dark areas remain unaddressed. The drawback to a random access scanner is the unavoidable time that one must wait before each new location can be addressed. Unlike raster scanners, a random access scanner must load the necessary electronic signals for each point each time it scans. This inherent access time ultimately limits the number of voxels that can be addressed. Both galvanometer mirrors and acousto-optic deflectors can be used in the random access mode but the access time for galvanometers (1 ms) is far too long to be useful for volumetric scanning. Acousto-optic (AO) scanners have effective access times that are 1000 times less. The next section will cover the design of this type of scanner as used in SSC San Diego's volumetric display.

3. LASER SCANNER SYSTEM

The FY 92 prototype 3-D volumetric display used an off-the-shelf, single-channel, 256 x 256 random access AO scanner (supplied by NEOS Technologies, Inc.) capable of addressing approximately 4,000 voxels at a 20-Hz refresh rate in a 13-inch-diameter helix. While this was adequate for some applications, the goal for FY 93 was to increase the number of voxels available for display.

Figure 1-3 shows a diagram of a single-channel AO deflection system. Basically, it consists of an AO intensity modulator followed by two AO deflectors for independent X and Y deflection. This system has an access time of 10 μsec, meaning that it takes 10 μsec for the acoustic wave to fill the aperture of each deflector and achieve the desired deflection of the laser beam to a new location. This implies a voxel rate of 1/(10 msec), or a maximum of 100,000 voxels per second. After allowing for a 20-Hz refresh rate, we are left with a 5,000 voxel, flicker-free image. The usable voxel rate is somewhat less than this, as some dwell time needs to be allocated for the laser beam at each location to have an image of any significant brightness. This scanner has an overall throughput efficiency of about 10% and represents the practical upper limit in off-the-shelf acousto-optic scanning technology. Attempting to go beyond this limit leads to decreased efficiencies and more complicated optical design.

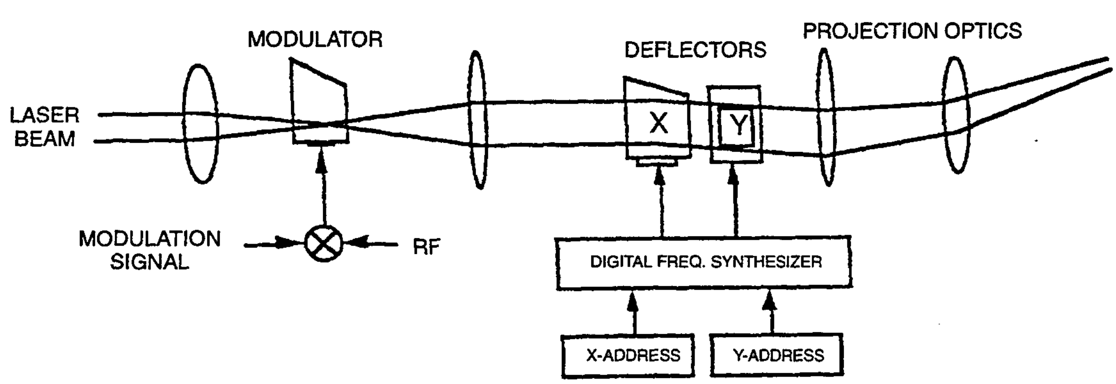


Figure 1-3. Single-channel scanner.

The most straightforward approach to increasing the number of voxels is to couple several scanners together in parallel. To achieve the target of 40,000 voxels, a four-channel system was designed and built by NEOS Technologies, Inc. It consists of four of the single-channel scanners described above packed into a single box (figure 1-4). By cutting the access time from 10 μsec to 5 μsec, the number

of voxels in each channel was doubled to 10,000, for a total of 40,000 voxels per frame at 20-Hz refresh. The lower access time was achieved by reducing the optical beam diameter in the AO deflectors from 6 mm to 3 mm.

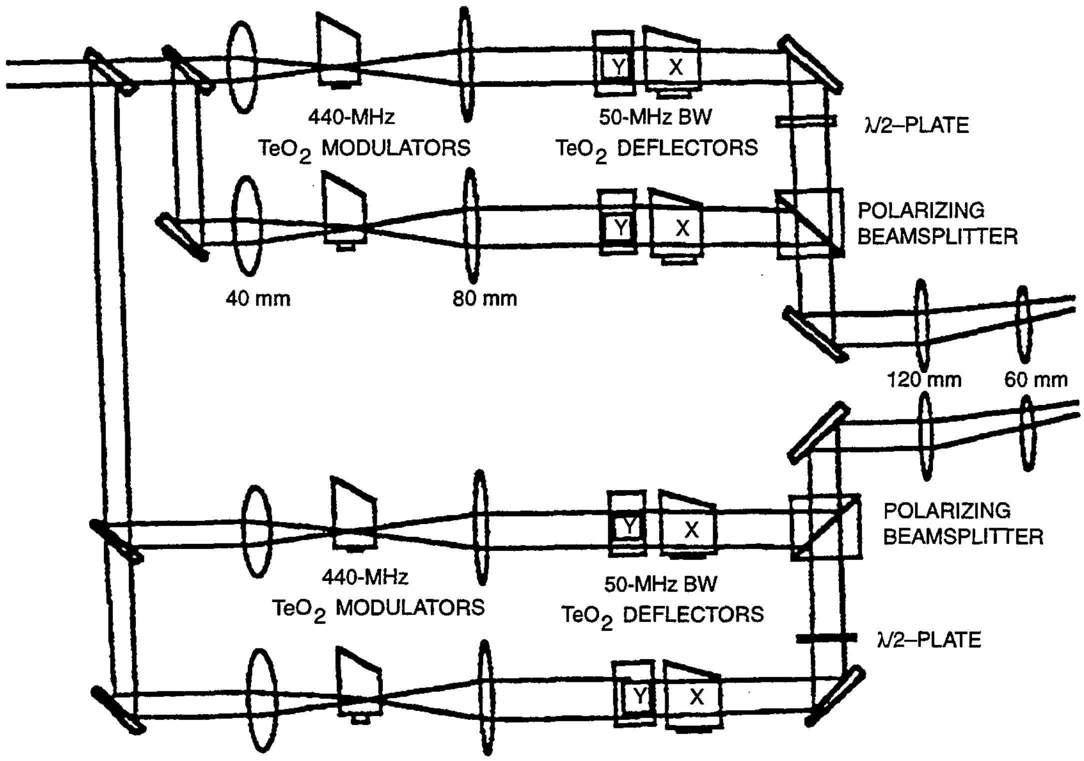


Figure 1-4. NEOS four-channel random access scanner.

Referring to figure 1-4, the laser input to the scanner is split four ways by beam splitters (channels A, B, C, and D). Each beam is then focused into a 440-MHz TeO_2 AO modulator. From there, the beams are re-collimated to a 3-mm diameter and sent to the X and Y TeO_2 AO deflectors. The deflectors are swept from 75 to 125 MHz in 5 μsec to achieve a time-bandwidth product of 250. Note that the positions of the X- and Y-deflectors are reversed in the four-channel system. This was done to optimize the polarization properties of the deflectors while maintaining a vertical polarization input beam to the scanner. The first-order beam from the deflector has its polarization rotated 90 degrees from the input beam. These deflectors require horizontal polarization at the input which, in turn, requires the Y-deflector to precede the X-deflector, if the initial polarization from the laser is vertical. This avoids the use of any waveplates to correct the incoming polarization.

The deflector outputs from two channels (A and B) are combined using a half-waveplate and a polarizing beamsplitter. This assures that both channels may be overlapped everywhere in the helix. The two outputs are then projected to the helix using the final output lens pair. The projection lenses also act to increase the angular magnification of the scanner by about a factor of 2.5. This helps reduce the required throw distance between the scanner and helix, while maintaining a reasonable spot size. Channels C and D are handled in a similar fashion. Performance of this scanner with the 36-inch helix will be covered in Section 5.

4. VOLUMETRIC DISPLAY SYSTEM—OPTICAL LAYOUT

The integration of the four-channel AO scanner described above with its electronics package and the 36-inch helix is shown in figure 1-5a. An argon–ion gas laser is used as the light source for the system. Laser powers in the range of 100 mW to 1 W have been used with no serious problems. Special care must taken to meet the input-beam-diameter requirement of 1.6 mm at the input to the scanner to achieve the desired spot size throughout the rest of the system. This is accomplished by moving the laser far enough away from the scanner, or through the use of up-collimating optics. It is also mandatory that the laser be run in single mode to produce a minimum spot size at the helix surface.

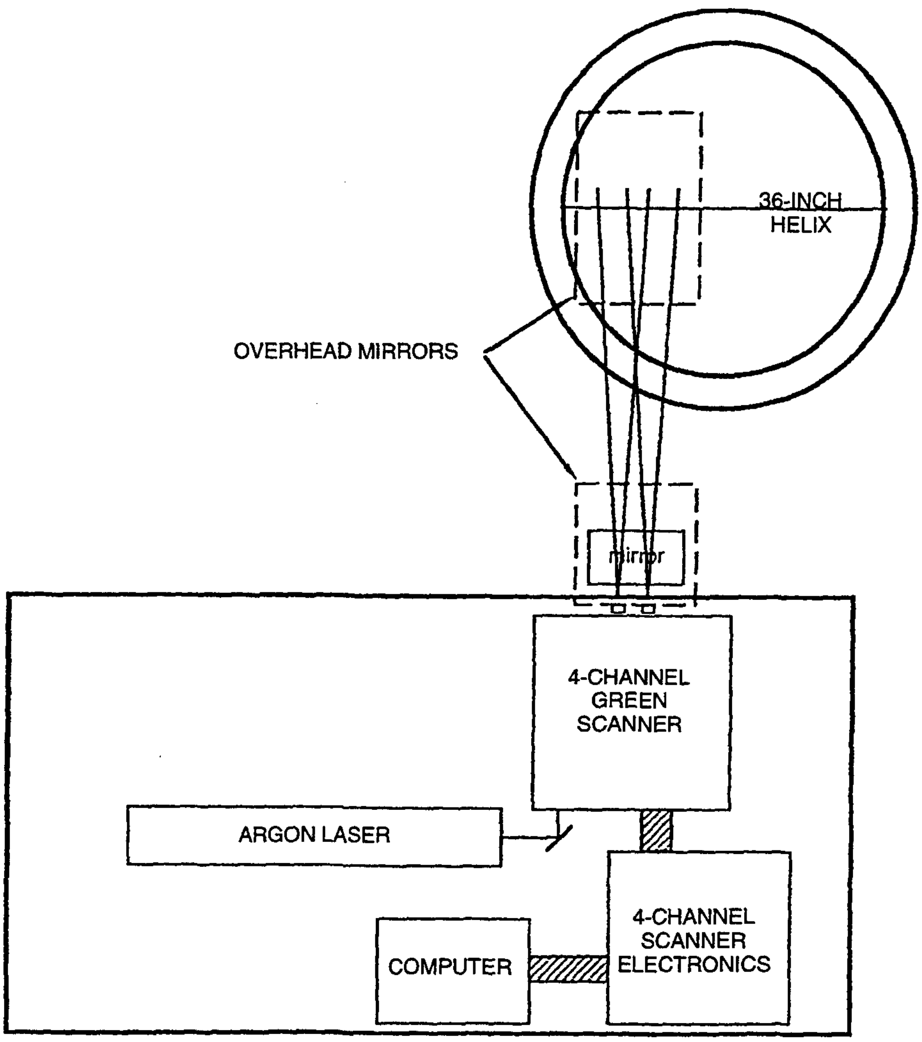


Figure 1-5a. Top view of laboratory setup for volumetric 3-D display (to scale).

The helix is mounted as a separate structure apart from the laser scanner with the display image being relayed by mirrors up into the ceiling and transmitted vertically downward onto the helix (figure 1-5b). The helix is 36 inches in diameter and 18 inches high. Details of its construction can be found elsewhere in Section 2. The electronics package consists of the rf drive and switching electronics and a custom interface board to route the image data from the host computer and sequence it to the proper channels in the scanner. The details of these components will not be discussed here, as they are found in other sections of this report.

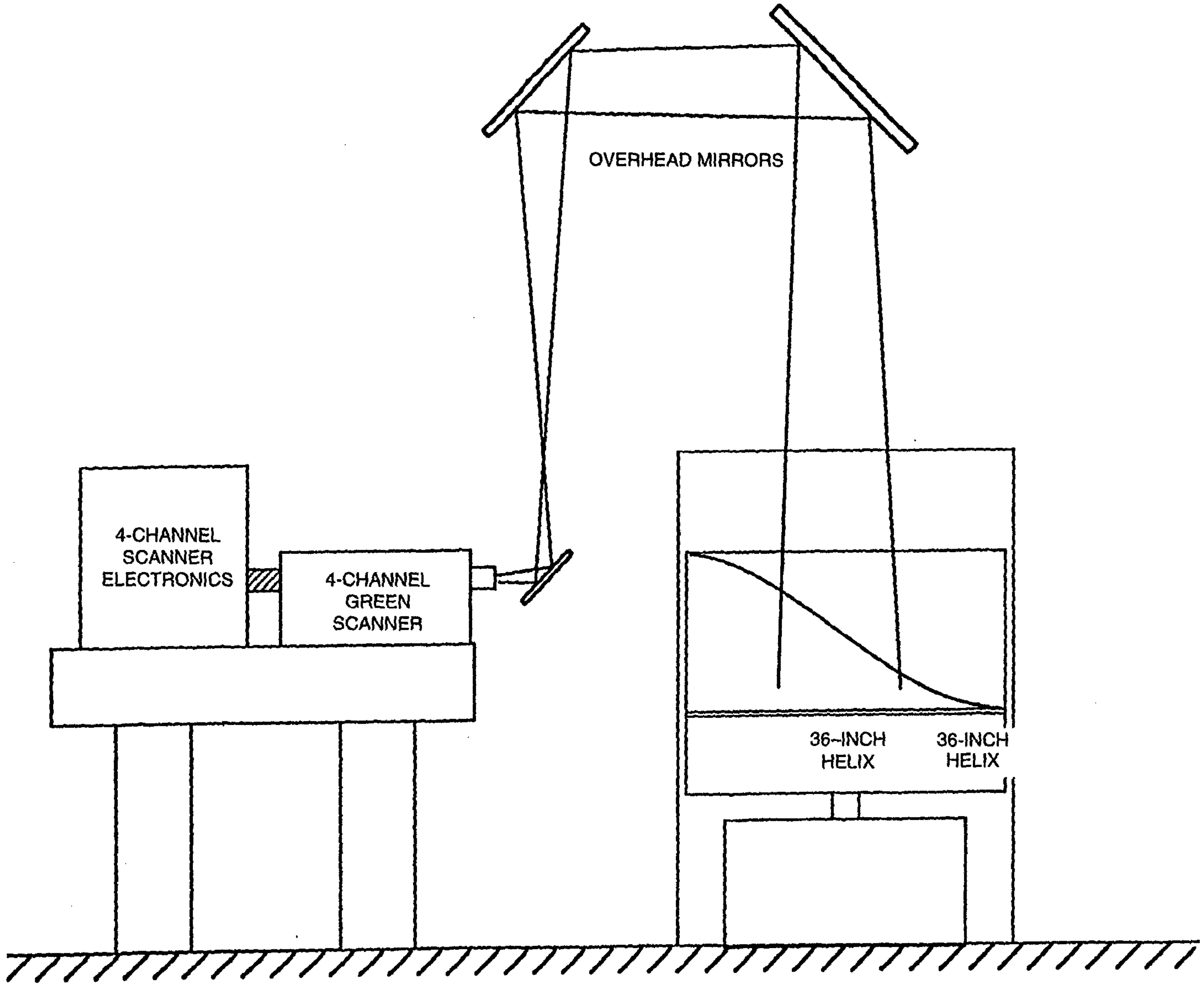


Figure 1-5b. Side view of laboratory setup for volumetric 3-D display (to scale)

5. SYSTEM PERFORMANCE

5.1. SPOT SIZE ANALYSIS

One of the objectives of the 36-inch system was to increase the effective display area without the voxel size becoming too large. The following analysis was used to explore various ways of achieving that goal.

We know the space bandwidth product for a given display system is an invariant. That is, for a given projection width and a fixed maximum number of pixels, the minimum spot size is roughly found by dividing the projection width by the pixel number. For a 24-inch width (610 mm) and 256 pixels, we get a pixel diameter of 2.4 mm.

We also know that for a given initial beam divergence angle θ, and laser beam waist diameter, *d,* there is another constant that we must contend with, namely,

$$\theta d = \frac{4\lambda}{\pi}, \tag{4}$$

where λ is the optical wavelength. This is another way of saying that lasers do not emit collimated beams of light. If one tries to reduce a beam's divergence by running it through a telescope, the beam's diameter must invariably grow in proportion. Likewise, if one attempts to decrease the diameter of a beam by running it through an inverted telescope (as is done in the NEOS scanner), then that beam's divergence must increase proportionately. This all results from the basic law of diffraction: the smaller the aperture, the larger the beam spread.

The half-angle scan range from an acousto-optic deflector is given approximately by

$$\Delta\theta = \frac{\lambda}{2v_s}\Delta f, \tag{5}$$

where Δf is the rf frequency sweep, v_s is the acoustic velocity, and λ is the optical wavelength. In the NEOS four-channel scanner, $\Delta f = 50$ MHz, and $v_s = 0.65$ mm/ms. Substituting these numbers leads to a total deflection angle of $2\Delta\theta = 0.0396$ rad = 2.27 degrees. With the 5x angular magnification from the output lenses used in the current system, this gives a total scan angle of 5 x 2.27 degrees = 11.4 degrees. Measurements indicate a 12-degree scan, in reasonable agreement with theory.

With this in mind, there are basically four ways to reduce the spot size on the 3-D helix. Figures 1-6 and 1-7 are scale drawings showing the previously used addressable area and the newly implemented system change showing the trade-offs in voxel size vs. image area. Figure 1-6 shows the addressed area of the previous system. Figure 1-7 shows the effect of reducing the 4095 x 4095 addressing area to fit more completely inside the desired viewing area. The basic idea is to make full use of the 4095 by 4095 addressable image area available to the 256 x 256 scanner, and to create the desired image size through changes in the optical system rather than software. Software corrections should be saved for fine tuning and color convergence.

Figure 1-8 shows a gaussian beam trace through one channel of the NEOS scanner showing the predicted spot size at the helix. The system is unfolded here for clarity. The approximate spot size calculation from above for the current system (2.4 mm) does not agree very well with the more accurate prediction from the gaussian beam propagation analysis (3.6 mm). This is because the rough calculation did not take into account the Rayleigh resolution criterion, which would have given a larger beam

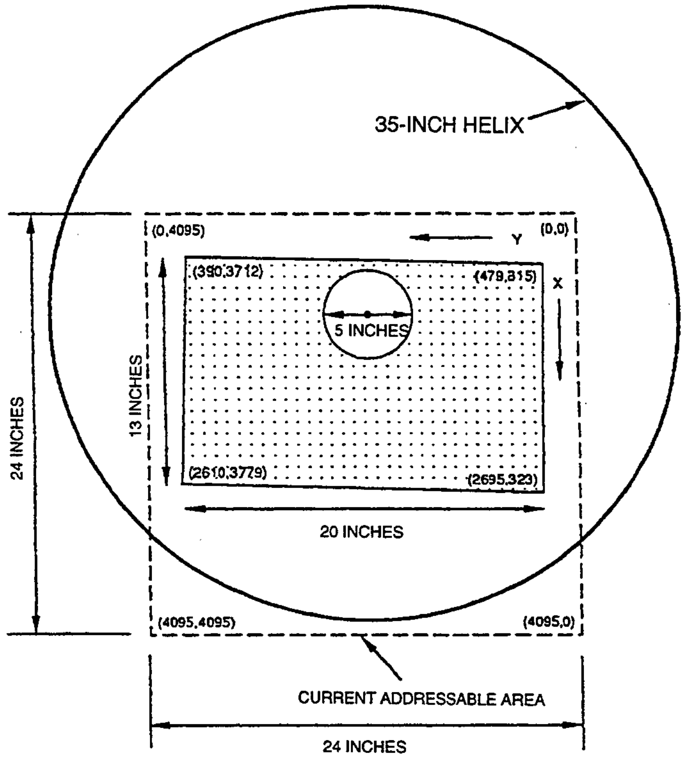
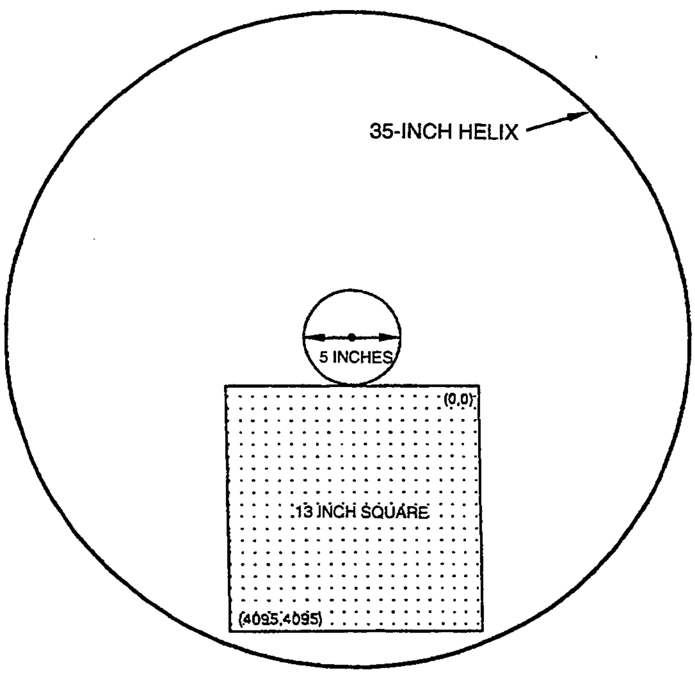


Figure 1-6. Previous helix addressability.



NEW VOXEL SIZE APPROXIMATELY 1/2 OF CURRENT SYSTEM

Figure 1-7. New helix addressability for minimum voxel size.

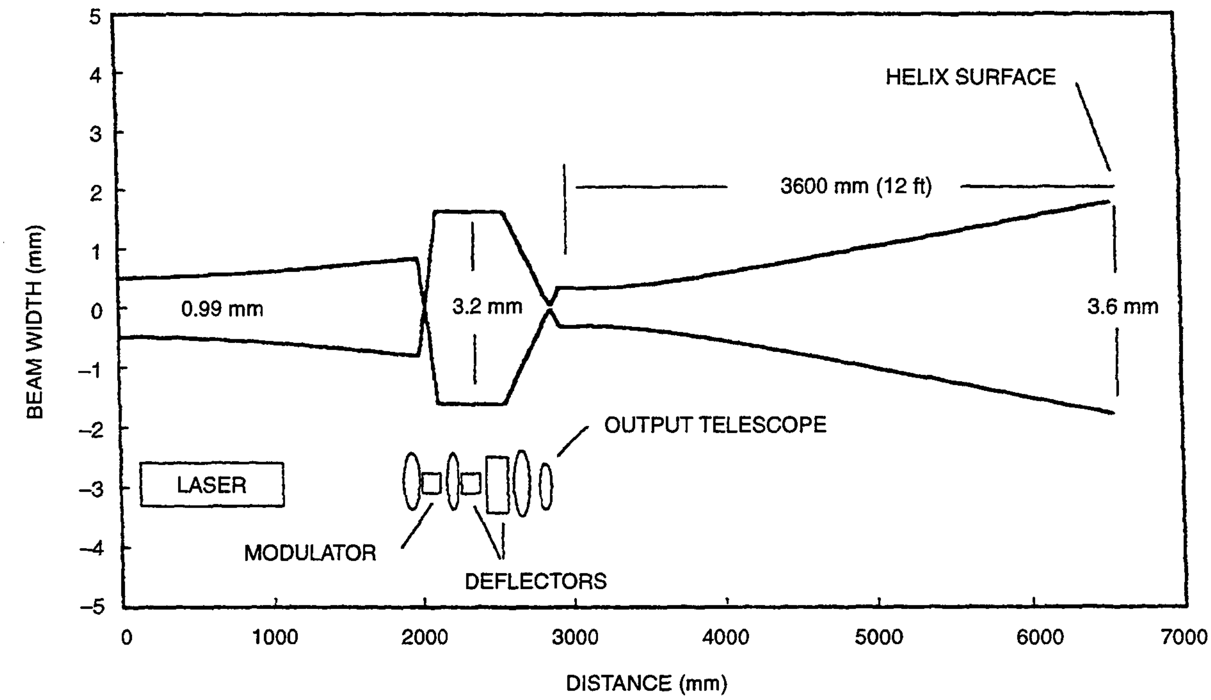


Figure 1-8. Gaussian beam ray trace of NEOS four-channel scanner.

diameter. The measured value of the spot size at the helix is approximately 4 $\pm$0.5 mm, in fairly good agreement with the gaussian analysis. Higher order lens aberrations probably increase the spot size over what a simple first-order gaussian ray trace would predict. Figure 1-9 shows the divergence of the Lexel argon laser all by itself, if it were allowed to propagate to the helix without the scanner optics. The spot size at the helix would be 4.26 mm. One can see here that we really do not improve things very much over the raw diverged laser beam.

Figure 1-10 is another view of the current scanner showing the deflection angle from the AO deflectors and the angular magnification from the output optics. If the output optics were removed and the laser beam from the deflectors (3.2 mm diameter) was allowed to propagate to the helix, then the beam diameter would expand to 3.3 mm (figure 1-11). In addition, without the output optics, the scan angle is reduced from 5.7 degrees to 1.13 degrees. Theoretically, the smallest spot size one could ever achieve would come from using a single focusing lens of 3600 mm (12 ft) as is shown in figure 1-12. A 0.74-mm spot diameter results with the resulting loss in scan angle. The maximum display area would be about 6 x 6, not a very desirable result.

We found that the spot size coming from the modulator is not a circular beam (approximately 3 mm x 6 mm). The 6-mm dimension is far too large for the required access time and also leads to diffraction lobes seen around the imaged voxels. We have installed apertures in the scanner that will produce a 3-mm beam to correct this problem. This, of course, means that we are throwing away some optical power. The beam should be circular upon exiting the modulator. This can be corrected by adjusting the input beam diameter to produce the proper spot size at the modulator.

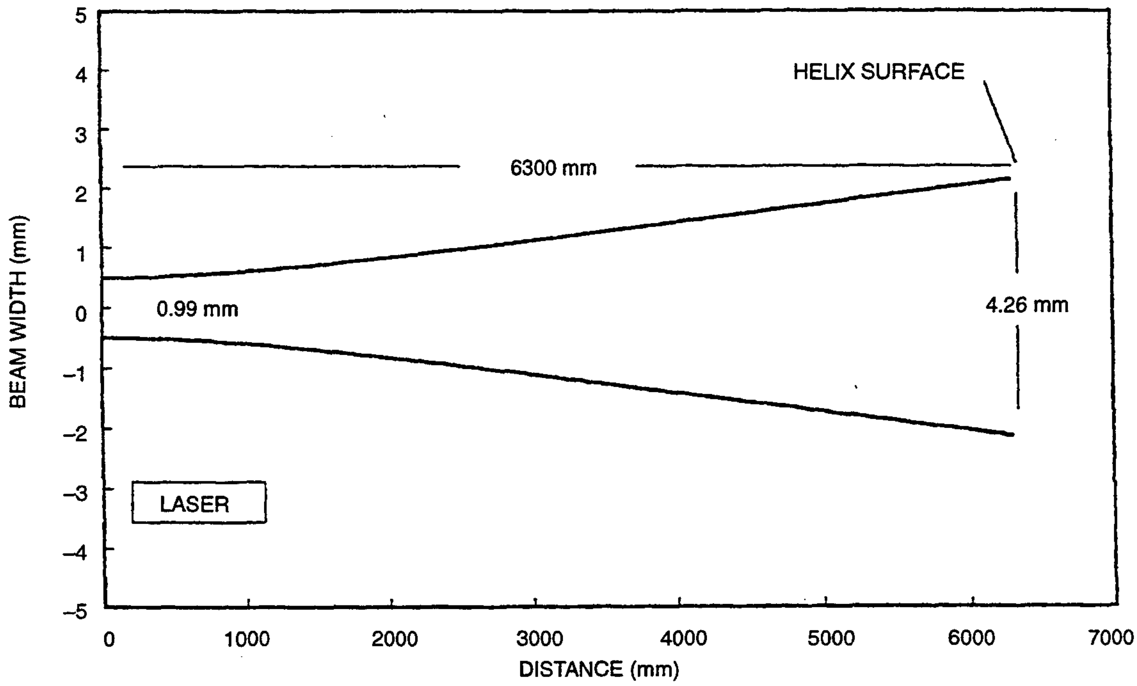


Figure 1-9. Gaussian beam ray trace of Lexel argon-ion laser.

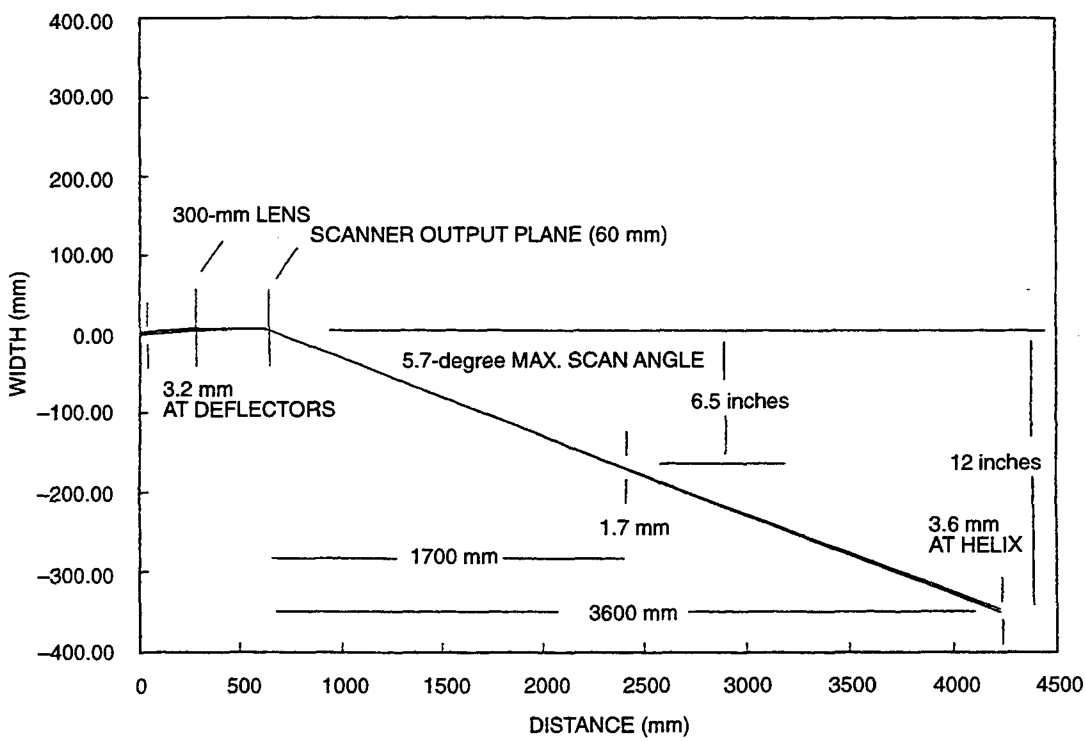


Figure 1-10. Gaussian beam ray trace of NEOS four-channel scanner output.

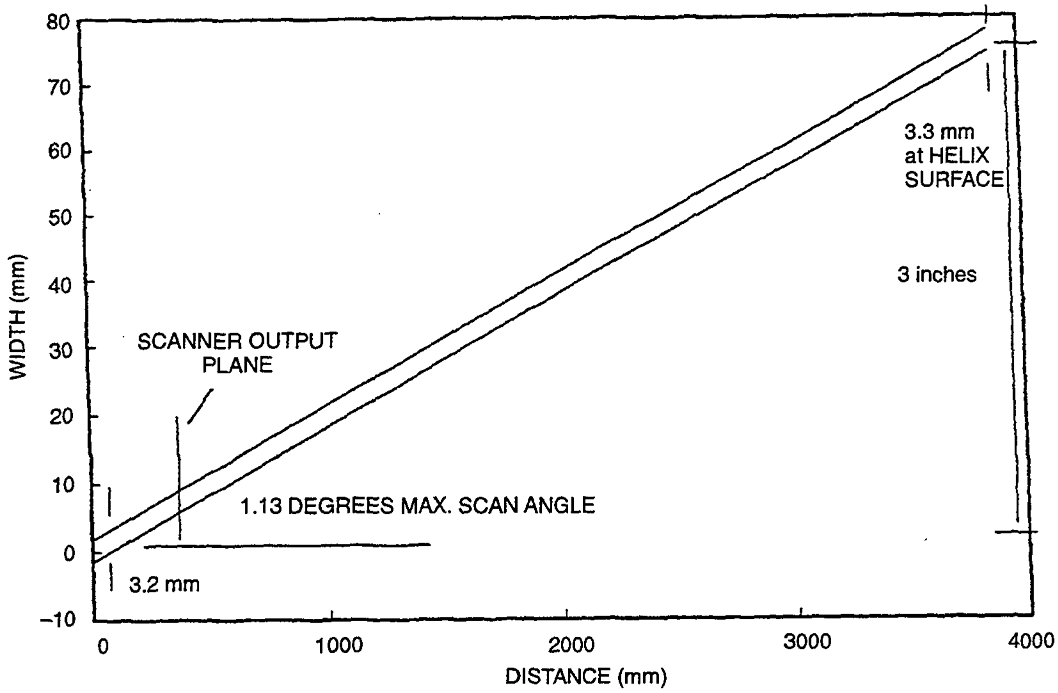


Figure 1-11. Ray trace of NEOS scanner output with no focusing optics.

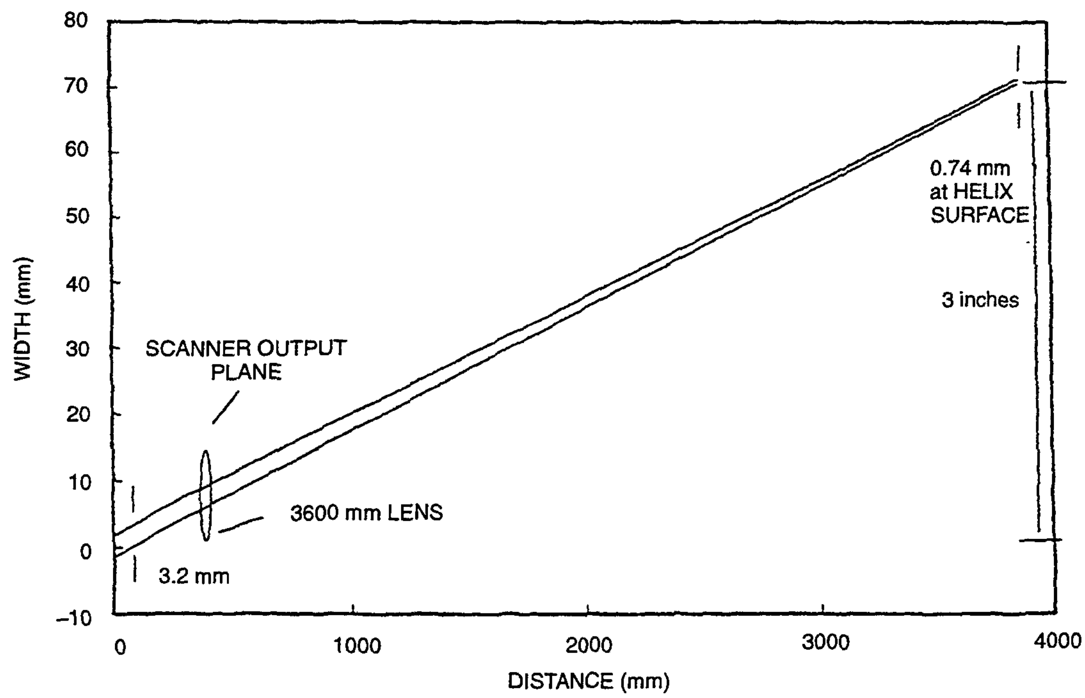


Figure 1-12. Ray trace of NEOS scanner output with 3.6-m focusing lens.

Figure 1-7 will be used here as a reference for the best spot size one could ever hope for on a 36-inch helix using the NEOS four-channel scanner. This means that we are essentially trying to reduce the addressable area by about a factor of two (24 x 24 to 13 x 13). Calibration software and correction EPROMs were reconfigured to accommodate the new dimensions.

The four methods of spot size reduction that were examined are outlined below.

Method #1. The most direct method to reduce the addressable area and, hence, the spot size, is simply to reduce the throw distance from the scanner to the helix. Figure 1-10 shows the effect of reducing the throw distance by approximately 1/2(1700 mm). A spot diameter of 1.7 mm results, with a correspondingly reduced image area of 13+ x 13+.

Method #2. Reduce the image size by using a single projection lens in front of the scanner. Figure 1-13 shows the effect of inserting 500-, 1000-, and 1500-mm lenses at various distances. This would undoubtedly introduce some aberrations in the image that might be difficult to remove. The best spot size is only 1.8 mm, greater than in Method #1. What is worse is that an 8-inch lens is required to achieve this spot size. This does not appear to be a viable solution.

Method #3. Use new output optics to decrease angular magnification and reduce the image size in the helix, while at the same time remapping the voxel images over the entire 4095 x 4095 address space. This means changing one or both of the output lenses in scanner. The best choice is to change the last output lens from 60 mm to around 110 mm (figure 1-14). The new spot size would be 1.7 mm.

Method #4. Last, but not least, one can increase the resolution of the scanner to create more spots in the same area (256 x 256 to 512 x 512). This essentially means increasing the beam size in the deflectors to 6.4 mm. The penalty for doing this is a proportional reduction in the total number of voxels from 40,000 to 20,000. Figure 1-15 shows a ray trace of this setup. A spot size of 1.8 mm is achieved at the helix with a 24 x 24 addressable area. If we optimize the addressable area to a 13 x 13 square, we could probably achieve sub-millimeter spot sizes.

Method #3 was chosen as being the most cost-effective and straightforward approach. After installing the 120-mm projection lens, the spot size at the helix was reduced from 4 mm to 2 mm.

5.2. EFFECT OF MISALIGNMENT

The effect on the spot size of a slight misalignment of the scanner optics is shown in figure 1-16. The 80-mm lens that collimates the beam coming from the modulator was shifted by ± 1 mm and the 60-mm output lens was moved in order to achieve the minimum spot size. It can be seen that the system produces essentially the same spot size as produced in the perfect collimation case (figure 1-7).

5.3. OPTIONAL CONFIGURATIONS

Using gaussian beam traces, additional analysis on different potential display volumes, helix sizes, and scan angles was done. The results are shown in figure 1-17a. The first column refers to the overall helix diameter. The second column shows a small graphical representation of relative position of the display volume when viewed from the top of the helix. Next to the graphic is the length of one of the sides of the scan area in inches. The third column shows the spot diameter obtained for both 5 degree and 10 degree scans. The fourth column indicates the needed throw distance to achieve the

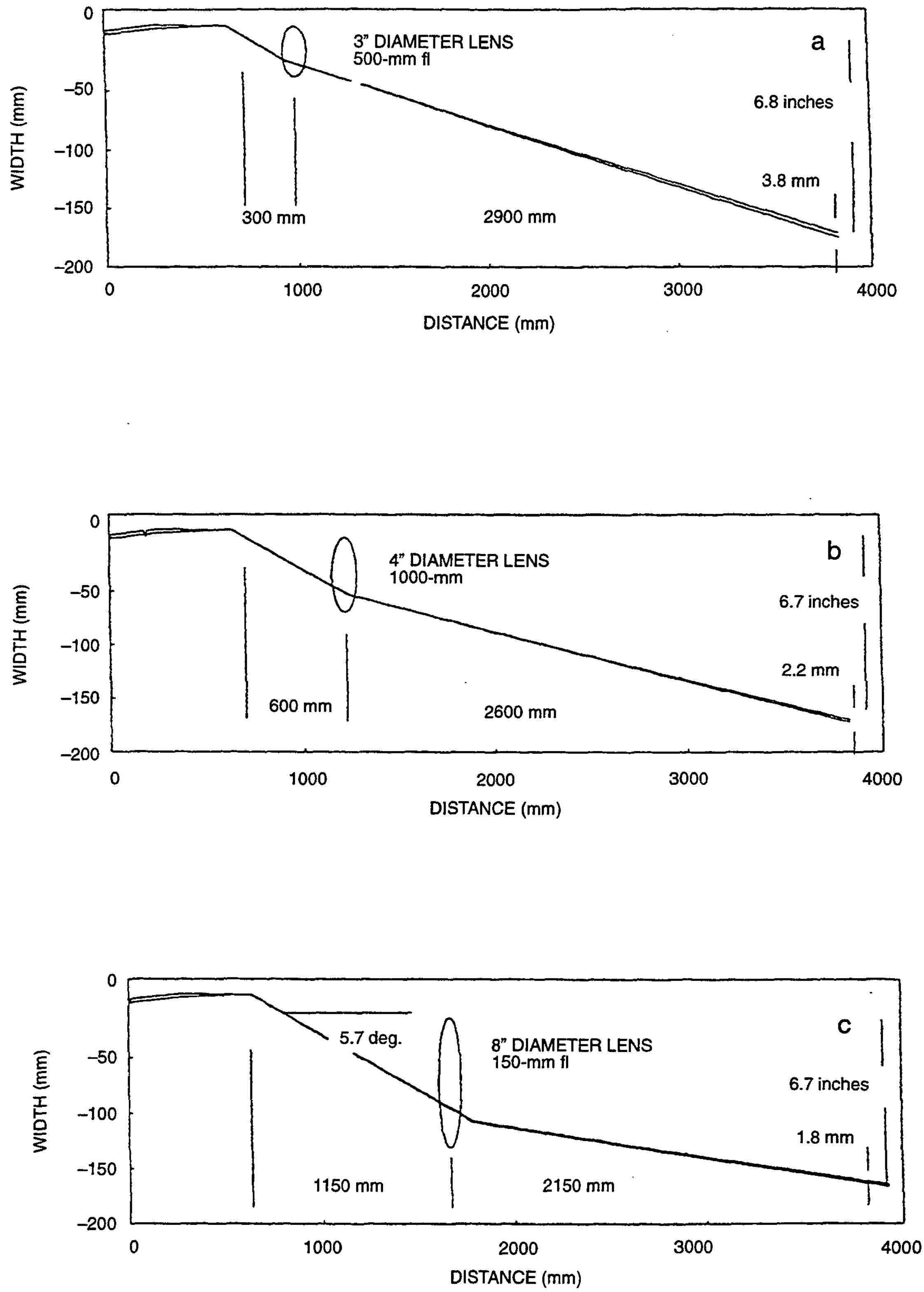


Figure 1-13. Ray traces of NEOS scanner output with (a) 500-mm, (b) 1000-mm, and (c) 1500-mm focusing optics.

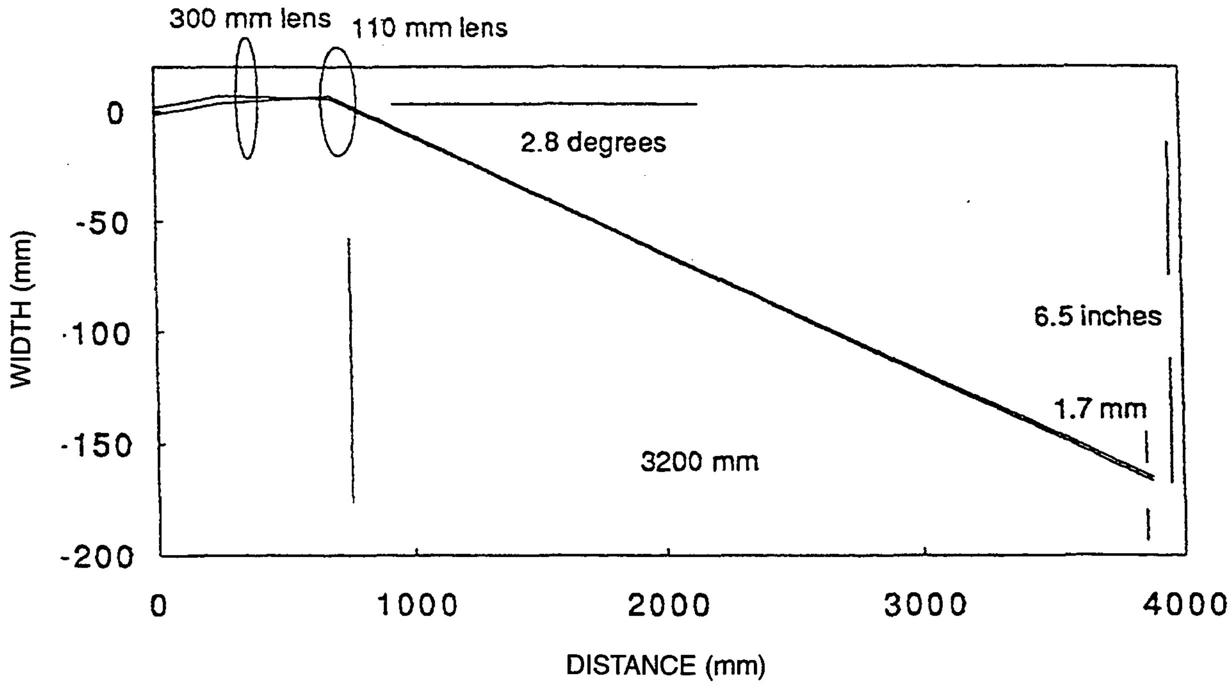


Figure 1-14. Gaussian ray trace of NEOS four-channel scanner with 2.5x telescope.

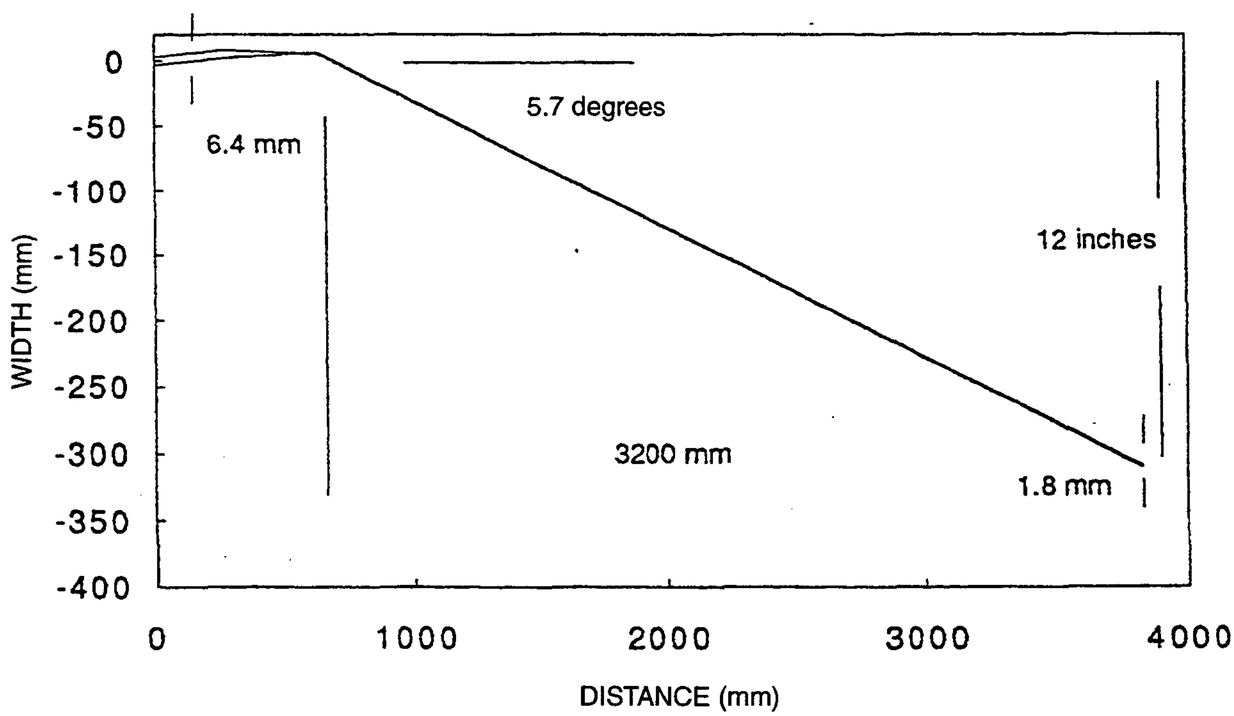
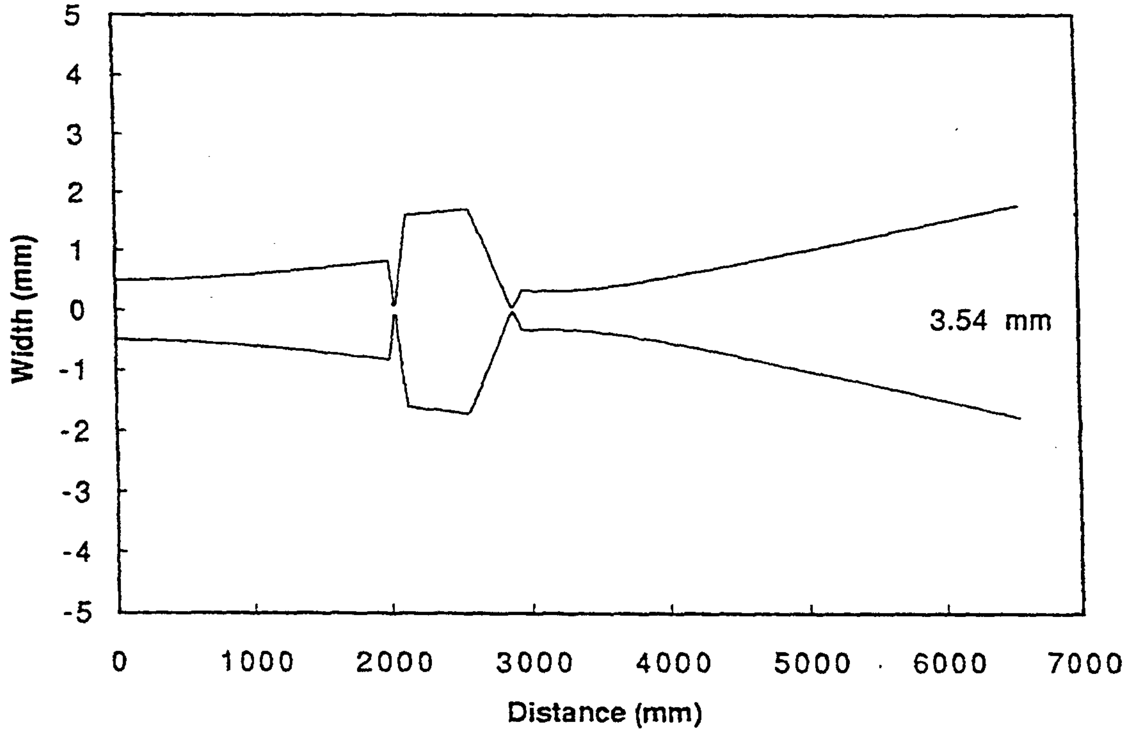


Figure 1-15. Gaussian ray trace of NEOS four-channel scanner with 512 resolution.



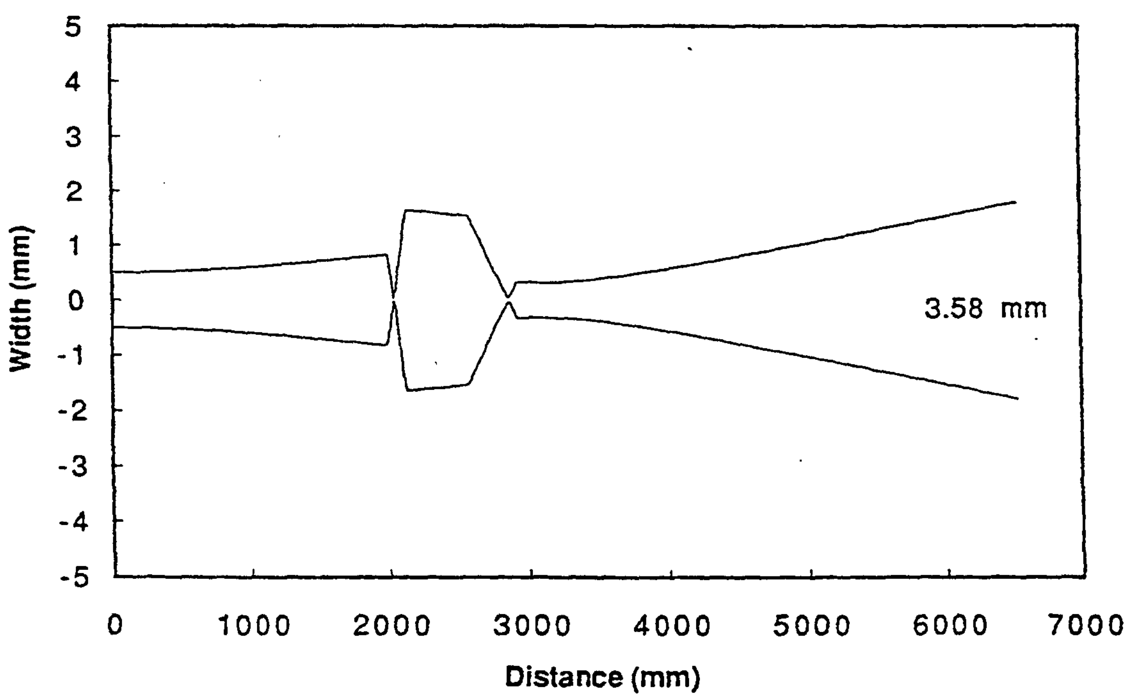


Figure 1-16. Gaussian ray trace of NEOS four-channel scanner showing effect of misalignment on spot size.

corresponding spot size from column three. Note the differences in throw distance for 5- and 10-degree scans. Figure 1-17b is also a graph showing the results of the second and fourth columns. It is also interesting to note that, for a given system, the spot size remains the same when one changes from a 5-degree scan to a 10-degree scan. This is because of the corresponding change in the magnification of the projection optics used to produce the required scanning dimensions.

5.4. EFFECT OF LASER DIVERGENCE

Figures 1-18 and 1-19 show the effect laser divergence has on the scanner spot size. Because we are collimating the beam at the deflectors, it makes little, or no difference what divergence is used for the input. A spot size of 3.6 mm is obtained, regardless. The 50-mrad divergence used for the laser divergence in figure 1-19 is not even available from any commercial laser and is shown here as an extreme example of a more or less perfectly collimated laser.

The effect of laser divergence cannot be totally ignored. The incoming beam diameter and divergence must be properly matched to the AO modulator inside the scanner. The next section covers the design procedure for this requirement.

5.5. ACOUSTO-OPTIC MODULATOR ANALYSIS

This section describes the issues involved in choosing between different modulators and how they affect the overall size and cost of the scanner. The analysis is based on the paper, "Design Procedure for Wide Bandwidth Acousto-Optic Modulator."

The key ingredient here is the R-factor, defined as the ratio of the acoustical beam spread to the incoming optical beam spread. R can be related to the eccentricity, or ellipticity of the outgoing first-order diffracted beam. From the paper, we have

$$R = \frac{n\pi V\omega_o}{2f_a\lambda_o L} , \tag{6}$$

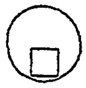
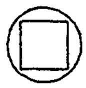
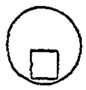
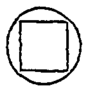
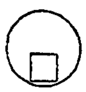
where n is the refractive index; V is acoustic velocity; ω_o is the optical beam radius; f_a is the acoustic center frequency; λ_o is the optical wavelength; and L is the transducer width. The values for the TeO_2 modulators we currently use are

$n = 2.26$
$V = 4.2$ mm/microsecond
$L = 0.67$ mm
$f_a = 440$ or 260 MHz
$\lambda_o = 442,514$, or 647 nm.

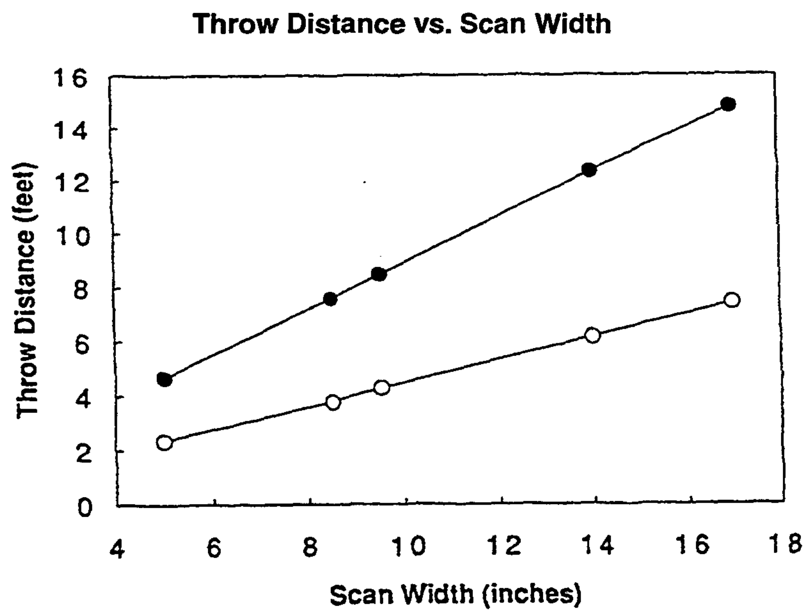
Putting these numbers in for the 440-MHz/514-nm case yields a simple relationship between R and ω_o:

$$R = 0.0983\,\omega_o . \tag{7}$$

NEOS Scanner Spot Size Analysis

	Scan Length (inches)		Spot Diameter (mm) 5 deg scan	Spot Diameter (mm) 10 deg scan	Needed Throw Distance (feet) 5 deg scan	Needed Throw Distance (feet) 10 deg scan
12-inch		5	0.7	0.7	4.6	2.3
12-inch		8.5	1.1	1.1	7.5	3.8
24-inch		9.5	1.2	1.2	8.4	4.3
24-inch		17	2.2	2.2	14.8	7.4
36-inch		14	1.9	1.9	12.3	6.2

(a)



(b)

Figure 1-17. Spot size and throw distance comparison for different display configurations.

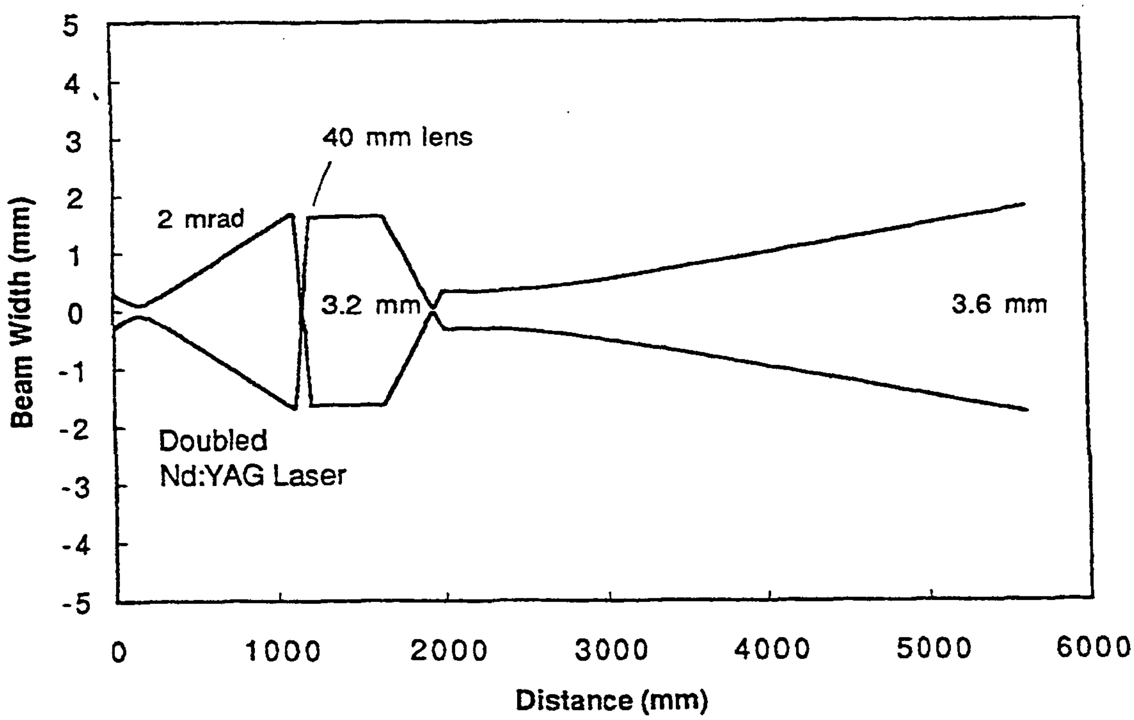


Figure 1-18. Gaussian ray trace of NEOS four-channel scanner with diode-pumped, doubled Nd:YAG laser.

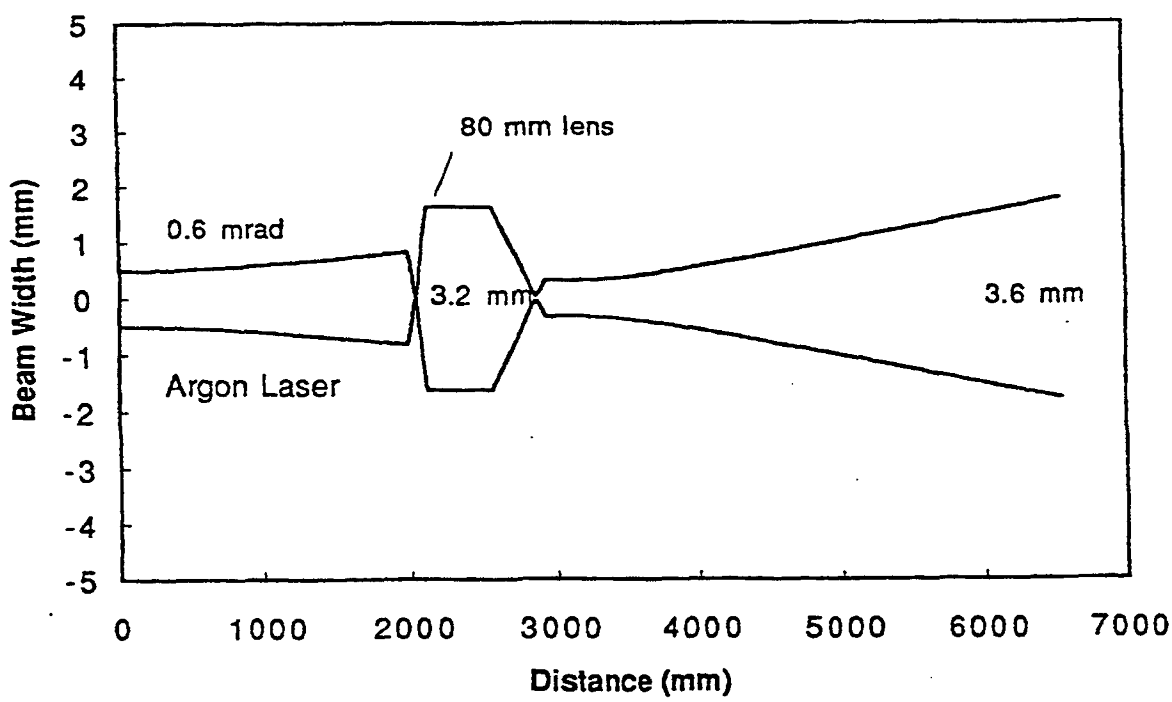


Figure 1-19. Gaussian ray trace of NEOS four-channel scanner with LEXEL argon-ion laser.

Figure 1-20 shows the graph of this line, as well as the relationships for the other wavelengths and the 260-MHz modulator. Optimal values for the *R*-factor are between 1.5 and 2.0. Figure 1-21 shows the relationship between the *R*-factor and the eccentricity. For optimal values of *R*, we see that the eccentricity of the first-order beam is between 0.90 and 0.95. The reason we do not seek an eccentricity of 1.0 (a perfect circle) is because this would imply an *R*-factor of around 6.0. According to the equation above, this means decreasing the center frequency, or increasing the spot size by a factor of 3 or 4, which is not very practical (i.e., loss of bandwidth).

At the other extreme, we also get an elliptical output (in the opposite sense) if the input beam overfills the acoustic beam, causing an aperturing effect in the vertical direction. This begins to occur for beams over 80 microns in diameter for the 440-MHz AOMs.

To analyze a given situation from a known spot size, one finds the R-factor in figure 1-20 and then reads off the eccentricity in figure 1-21. For our case of the Lexel argon laser (514 nm) and the 440-MHz modulators in the four-channel green scanner, the spot size at the modulator is estimated to be 16 mm. This gives R = 0.8 and an eccentricity of 0.75, or a beam diameter ratio of dx/dy = 3/4, a reasonable value. With the Laser Ionics argon laser, we have a larger spot size at the entrance to the scanner, which translates into a smaller spot size at the modulator. We are observing a beam eccentricity of about 1/2. This would imply an R = 0.5 and a spot diameter of about 10 to 12 microns. This agrees fairly well with calculated estimates.

From figure 1-20, the optimal values for the 440-MHz modulator are between 25 to 50 microns, while for the 260-MHz modulator they are between 15 and 30 microns. Thus, the 260-MHz modulator is better able to handle a small diameter beam and still deliver good eccentricity and bandwidth. The downside is that the smaller spot size causes a greater divergence of the exit beam from the modulator. Coupled with the smaller deflection angle of a 260-MHz modulator means it is more difficult to separate the zero order from the first order. This is the reason NEOS put 440-MHz modulators in the green scanner.

The other design criteria for the four-channel scanner is the requirement that the beam entering the X-Y deflectors be 3.2 mm in diameter to achieve a resolution of 256 spots. If we assume a spot size at the modulator, we can calculate the beam diameter and separation from the zero order for a given set of lenses.

Figures 1-22 and 1-23 show some examples of this analysis for 440- and 260-MHz modulators using gaussian beam propagation techniques. The left-hand side of the graph is at the beam waist in the modulator. Both the zero and first-order beams are shown propagating to the 80-mm lens and then being collimated. Figure 1-22a represents our current green scanner with its 440-MHz modulator and 22-μm spot size. Figure 1-22b shows what happens if a 260-MHz modulator were to be used with a 22-μm spot size. As expected, there is little separation between the two beams. The situation is proportionally worse for blue wavelengths because of the wavelength dependence of acousto-optic deflection. For the time being, the 440-MHz modulators will continue to be used in the green scanner, instead of changing to the less expensive 260-MHz modulators.

The case for the red scanner is shown in figure 1-23. It shows the results for the 440-MHz and 260-MHz modulators with the 647-nm red wavelength, where the "ideal" R-factor is used for optimum eccentricity (R = 1.75). This implies an optimum spot size value of 45-μm for the 440-MHz modulator and 27-μm for the 260-MHz modulator. The problem here (as well as in the green scanner) is that the ideal spot size does not diverge rapidly enough to reach the required 3.2-mm beam

diameter at the collimating lens. To compensate for this, a longer focal length lens must be used. Therefore, the next-generation red scanner will end up being 5 to 10 inches longer. The green scanner will remain the same size by utilizing its internal space more efficiently.

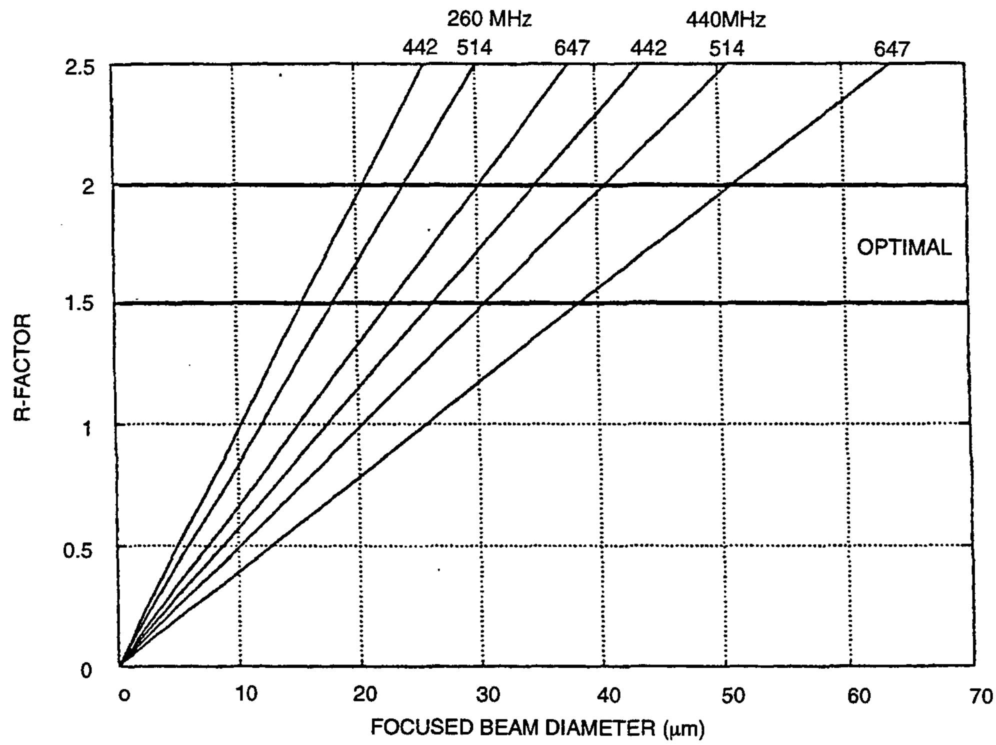


Figure 1-20. The *R* factor.

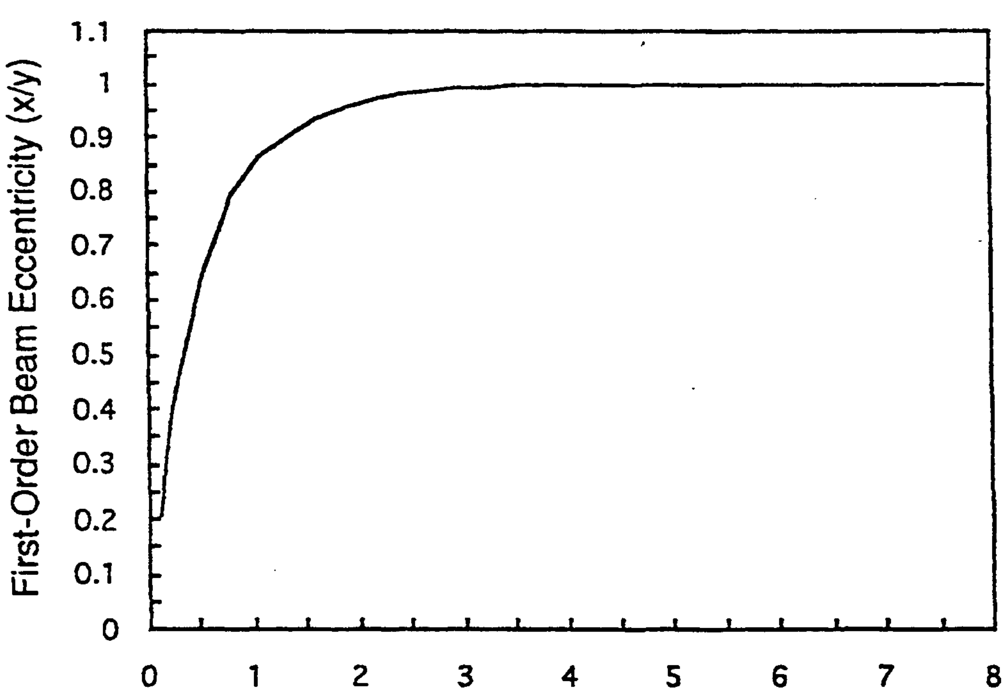
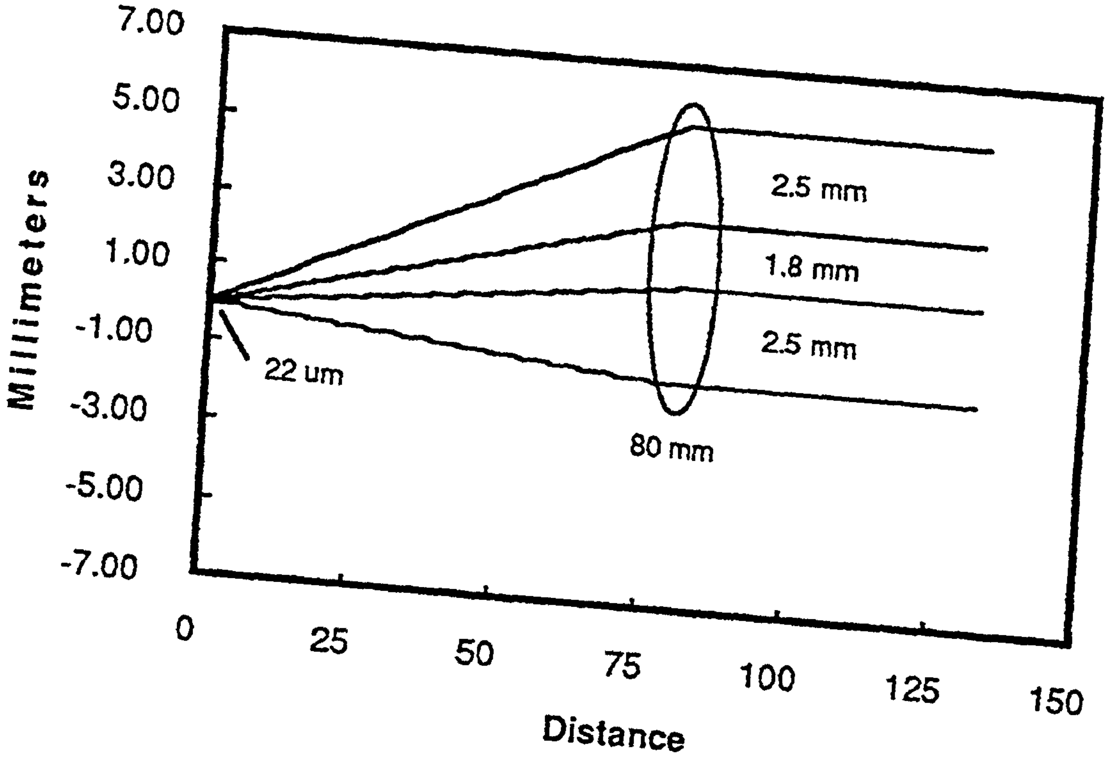
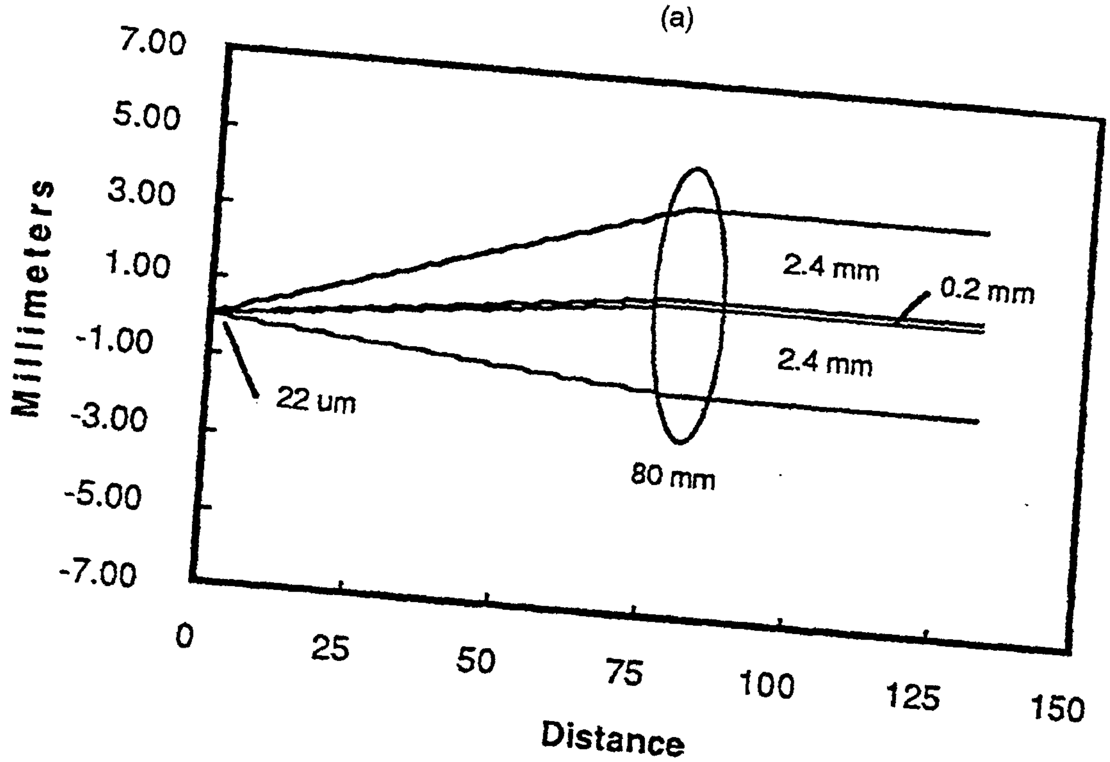


Figure 1-21. The *R*-factor eccentricity.



(a)



(b)

Figure 1-22. Zero/first-order beam separation using 514-nm laser light for (a) 440-MHz and (b) 260-MHz modulators.

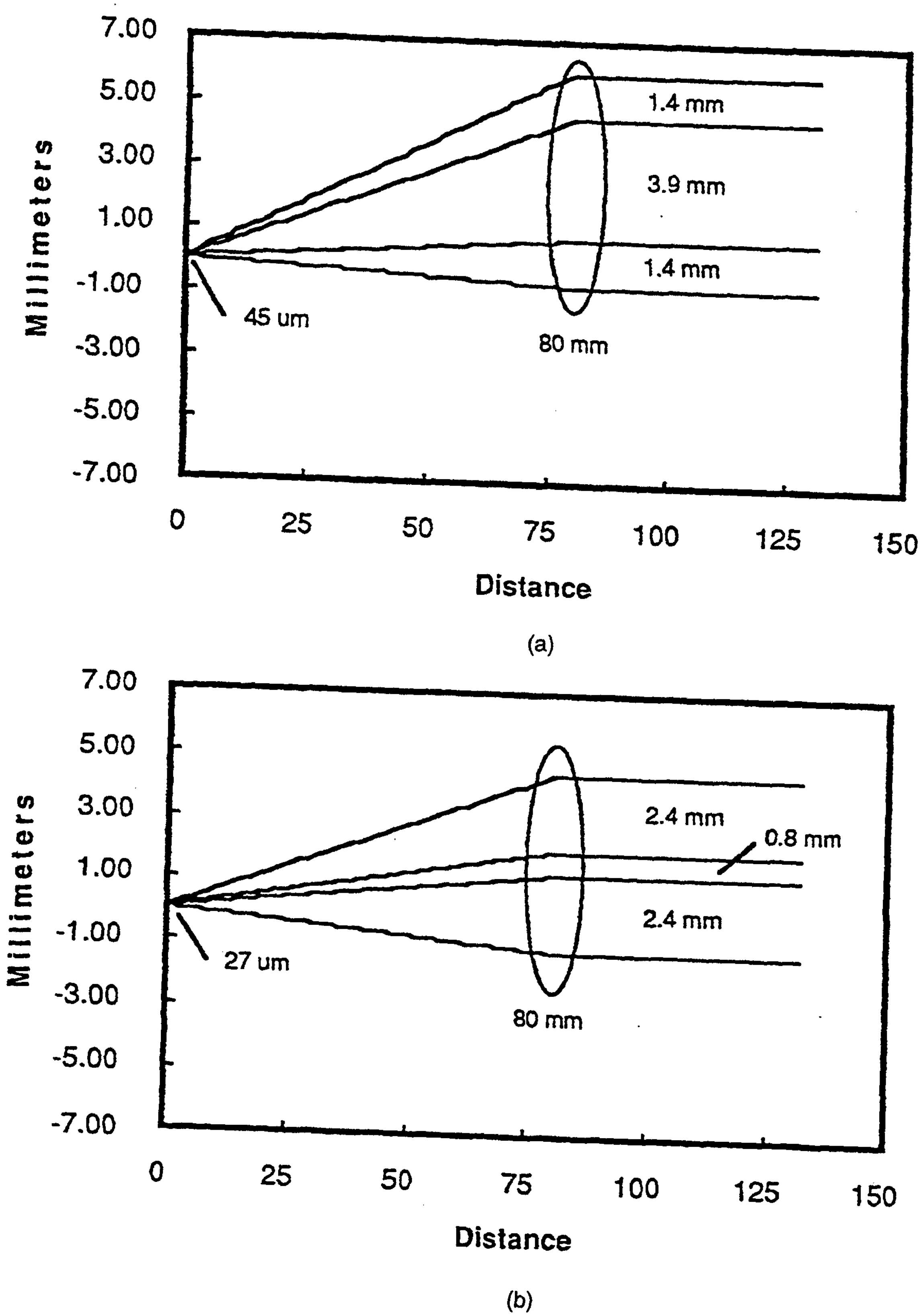


Figure 1-23. Zero/first-order beam separation using 647-nm laser light for (a) 440-MHz and (b) 260-MHz modulators, using optimal initial spot sizes.

5.6. LASER EVALUATIONS

Input laser powers from 100 mW to 1 W have been used with the green scanner with no noticeable problems. The real optical efficiency of a random access scanner depends on the voxel on-time needed for a given number of voxels. With an overall optical efficiency of 10%, time-average output powers for the scanner are on the order of 10 to 15 mW for an input of 150 mW. Of course, because of the finite access time, the actual scanner output intensity is a function of the number of voxels being displayed. The more voxels displayed, the less efficient the scanner becomes. Data for two different situations are shown in table 1-1.

Table 1-1. Number of voxels and scanner efficiency.

Number of Voxels	Total Average Image Power	Average Power Per Voxel
19,271	12.5 mW	649 nW
38,542	0.31 mW	8 nW

This implies an average power of less than a microwatt per voxel, which is well within safety guidelines.

To get some idea of the display brightness, we can calculate the number of foot-Lamberts (fL) coming from the scanner. We know that,

$$1fL = \left(\frac{1}{\pi}\right)\frac{\text{lumens}}{\text{ster}-\text{ft}^2}\,. \tag{8}$$

If we assume a solid angle of 2π steradians we can write

$$1fL = \left(\frac{1}{\pi}\right)\frac{\text{lumens}}{\text{ster}-\text{ft}^2} \times \frac{1}{0.7 \times 683\frac{\text{lumens}}{\text{Watt}}} \times 2\pi\ \text{ster} \times \frac{1ft^2}{92,903m^2} = 22\frac{nW}{mm^2}\,. \tag{9}$$

The factor of 0.7 is used here to account for the 5 14-nm laser wavelength instead of the 555-nm peak of the photopic curve. For a spot diameter of 2 mm at the helix, we have an approximate luminance from the scanner of

$$\frac{649nW}{\pi \cdot 1mm^2} \times \frac{1fL}{22\frac{mW}{mm^2}} = 9.4fL \tag{10}$$

for the 19,271 voxels case, and

$$\frac{8nW}{\pi \cdot 1mm^2} \times \frac{1fL}{22\frac{nW}{mm^2}} = 0.1fL \tag{11}$$

for the 38,542 voxels case. A typical CRT luminance in the green is about 20-30 fL. The display is usually operated under a low ambient to avoid seeing the white surface of the helix, so that these luminances are adequate for demonstrating the system.

One of the major criteria in achieving a truly compact and portable display is to find a way to eliminate the argon and krypton lasers. Our previous experience with solid-state lasers leads us to question whether or not these lasers are stable enough for display applications. Arrangements were made with two laser companies to loan us their diode-pumped green YAG lasers to help determine if they are suitable for the 3-D helix systems. Measurements were conducted on the current four-channel scanner

to determine the minimum requirements for laser power and voxel number, as well as stability and mode quality of the YAG lasers. Laser Diode Inc. and Coherent have sent their systems for evaluation. Figure 1-24 shows the stability of the two lasers over a 40-minute time period. The spikes in the curves are due to a defective power meter and are not real. The Coherent had virtually single spatial mode performance while the Laser Diode Inc. laser had definite inhomogeneities. The Coherent package was clearly superior in design compared to the Laser Diode Inc. model. Experiments conducted on the current four-channel scanner showed a reasonable brightness (with very low room lights) for both lasers tested. The superior mode quality and smaller beam diameter of the Coherent compensated for its lack of power.

Table 1-2 shows critical specifications for various laser systems and their potential use in 3-D helix systems. There is universal agreement concerning water-cooled gas lasers. Their one big advantage is output power, but a heavy price is paid in their wall-plug inefficiency. For 24- or 12-inch helix designs, we probably do not need that kind of power. But keep in mind the translucent plastic designs will require more power than the white reflective paint designs. On the 36-inch helix it appears that 200 mW is a minimum power requirement with the four-channel scanner. For the 24-inchtranslucent model that power requirement could stay about the same, although we do not really know yet. It is suggested that a small 12-inch translucent model be built first before going to the 24-inch.

Table 1-2. Lasers for display applications.

Color	Laser	Power	Comments
RED	Krypton (water-cooled)	>1 W	Water-cooled
	Krypton (air-cooled)	100 mW	Not enough power?
	Diode (single mode)	25 mW	One per channel
	Diode (multimode)	500 mW	Many unknowns
GREEN	Argon (water-cooled)	1 W	Water-cooled
	Argon (air-cooled)	100 mW	Not enough power?
	Doubled YAG (air-cooled)	250 mW	Somewhat expensive
BLUE	Argon (water-cooled)	>1 W	Water-cooled
	Argon (air-cooled)	100 mW	Not enough power
	Helium-Cadmium	130 mW	Somewhat expensive
	Solid State	60 mW	No commercial vendors

RED. Much excitement has been generated by the new red diode lasers. It is definitely the wave of the future. But keep in mind that last word, FUTURE. The "laser pointer" has fairly good beam quality due to its single-mode spatial characteristic, as well as its relatively few longitudinal modes. This means that it is fairly easy to collimate into a low divergence beam that can go through an X-Y acousto-optic scanner and be focused to a tight spot. The power of these diodes is running around 15 to 25 mW after going through the beam correction optics. We have demonstrated that this is just about enough power for a small helix (10,000 voxels), although a little more would probably be nice (or a shorter wavelength). As far as the four-channel scanner goes, one would have to put a single diode in each channel of the scanner. Direct modulation of the diodes is possible and would eliminate the need for any AO modulators, thereby improving efficiency. In addition, the system would be more compact because no special focusing optics are required as with the modulators. Also, there is no external laser to couple, so alignment would probably be more stable.

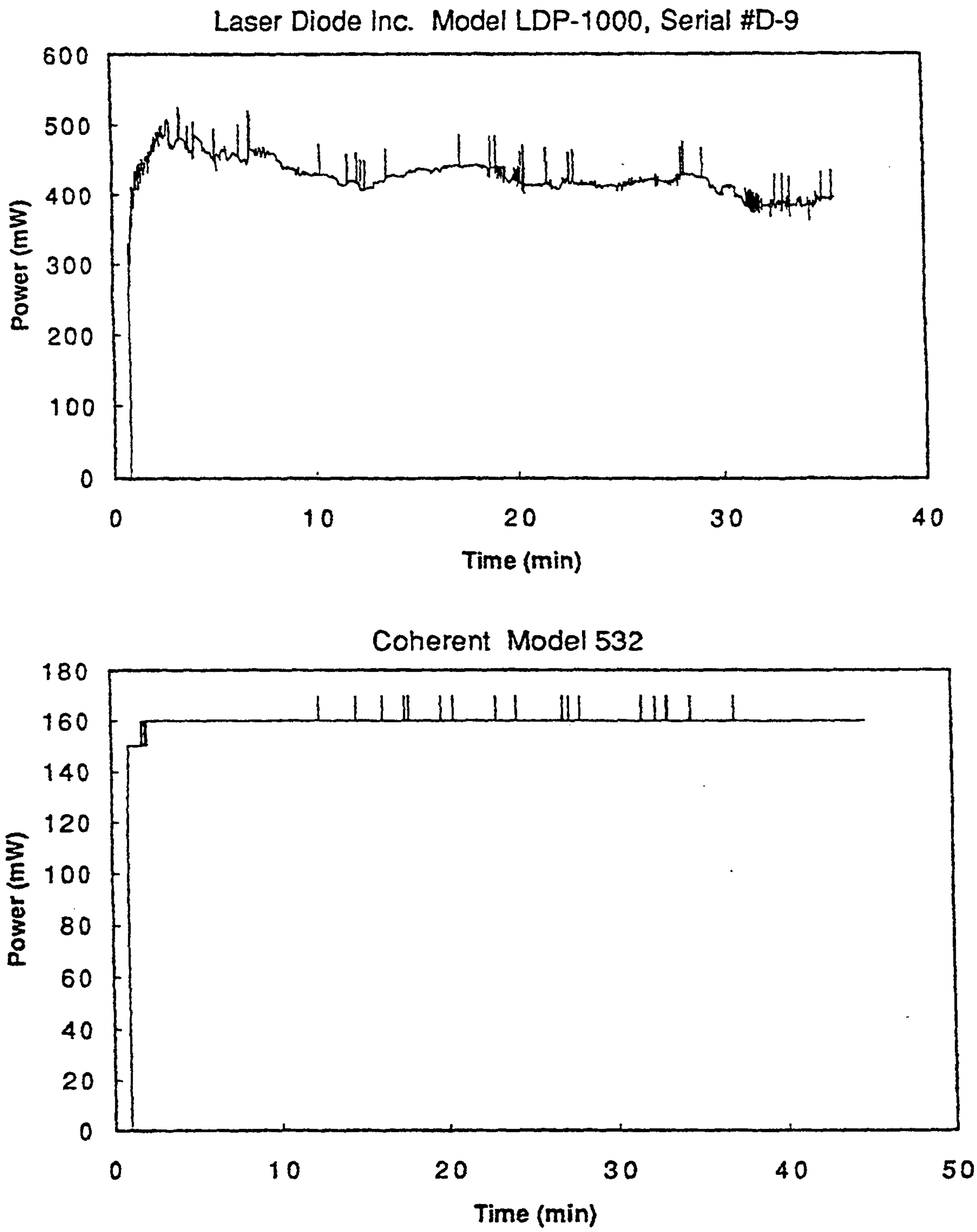


Figure 1-24. Output stability of two commercial diode-pumped YAG lasers.

The 500-mW diode is a completely different story. The way that this diode gets its power is by greatly increasing the size of the lasing aperture. Instead of a fairly symmetric 2- to 3-micron aperture, we now have a 100 x 1 micron aperture! This means many, many high-order spatial modes in the output beam. There are all sorts of problems in trying to get this kind of laser to be well-collimated without losing about half of the initial power. We have contacted a few companies who are willing to build a custom housing that will hopefully get the beam quality we desire ($2,000). But they have some reservations as to how successful they will be. This laser also has a much broader lasing spectrum (1 to 2 nm) which means it will probably not go through AO deflectors as well as other lasers. The other unknown is how well can you modulate one of these diodes (i.e., extinction ratio).

If we lose half the power, then we are down to 250 mW. This is great for a single-channel scanner. The question for the four-channel scanner is would it be better to use four single-mode diodes at an effective power of about 130 mW, or 1 multimode diode at 250 mW. We will not really know the answer until we do more experimentation with these diodes.

GREEN. The most popular choice for the green laser for just about any system is the doubled, diode-pumped YAG from Coherent. At 250 mW (perhaps 500 mW soon), it has adequate power and excellent beam characteristics. The only negative is the price: >$30 K. The most one can expect from an air-cooled argon is 100 mW, for $10 K, with a shorter lifetime.

BLUE. Compact blue lasers have always been a problem. While there is some work being done in the diode arena, the powers are milliwatts or less, and the lifetimes are days or hours. Any high-power blue diodes that we could use would probably be of the broad area kind like the red diode just described.

Solid-state blue sources in the tens of milliwatts range are in the laboratories, but none are being marketed. We could probably have one of these laboratories build a custom design to demonstrate the capability, but there is no estimate of the cost.

The only remaining alternatives are the argon and the helium-cadmium (HeCd) lasers. Most people in the laser-light-show business use the big water-cooled argons to get blue. Of course, the strongest blue line in the argon is the 488-nm line. Because this is an unacceptable blue from a chromaticity standpoint, the other deeper blue lines from the argon will be mixed to get an acceptable color. However, because we use AO scanners and can only use one laser line per color, this option is not open to us. An acceptable blue from the argon would be the 465-nm line. Unfortunately, there is not very much power in this line even in water-cooled systems. This basically says that a good blue for display color mixing purposes cannot be had from an argon laser.

For the moment, this all points to the air-cooled HeCd laser as the choice for blue. At 442 nm, it is definitely "too blue" by chromaticity standards. The eye does not respond too well at this wavelength, although our tests indicated that it can be used in our scanners with good results. The only real strikes against it are its size (5 feet long) and cost ($25K).

5.7. CONVERGENCE ANALYSIS

Convergence of the four channels from the scanner everywhere inside the helix is perhaps our most challenging problem for the immediate future. Figure 1-25 shows a scale drawing of the big helix optical system with the overhead mirrors removed for clarity. Here we are only looking at the x-axis, where most of the distortion occurs because of the separation of the two output lenses in this direction. This creates two pyramidal scanned sources that we must intersect everywhere inside the helix.

The problem is, if left alone, these two sources will only intersect at one location (the top of the helix in figure 1-25). They have separated by about 10 mm at the bottom of the helix. The necessary correction varies linearly across the scan. For channels C and D, there is no correction at, for example, the beginning of the scan, while there is a 10-mm correction at the end, while the opposite is true for channels A and B. If we want absolutely vertical lines in the display, there would be a slight correction even at the beginning of each scan. This correction also varies linearly from the bottom to the top of the helix where the pyramids intersect (figure 1-26). A similar situation results if we choose to intersect the pyramids at the bottom of the helix.

What about the y-axis? To get a better orientation of the situation, some computer simulations of two intersecting pyramids were made. In figure 1-27 there is an exaggerated example to illustrate the effect on the y-axis. It shows a small error in the overlap of the two pyramids in this direction. What does the actual intersection region look like? Figure 1-28 shows an intersection plane of the pyramids in the exaggerated case. One can see that it is not technically a nice, square plane. In addition, the shape changes as one moves perpendicular to the intersection plane. The good news is that this may not be too severe a problem. Figures 1-29, 1-30, and 1-31 show the actual 36-inch helix system. In particular, figure 1-26 shows the intersection planes at the top and the bottom of the helix. The error in the y-axis is barely detectable. It is clear that our main concern is with the x-axis convergence, and the y-axis can probably be ignored, which greatly simplifies the whole convergence process. If we are lucky, we might be able to do one correction at the bottom and calculate for the rest. Although, if we want perfectly vertical lines in the display, both A/B and C/D channels would have to be corrected in the y-direction. Having convergence and having vertical lines are two separate issues.

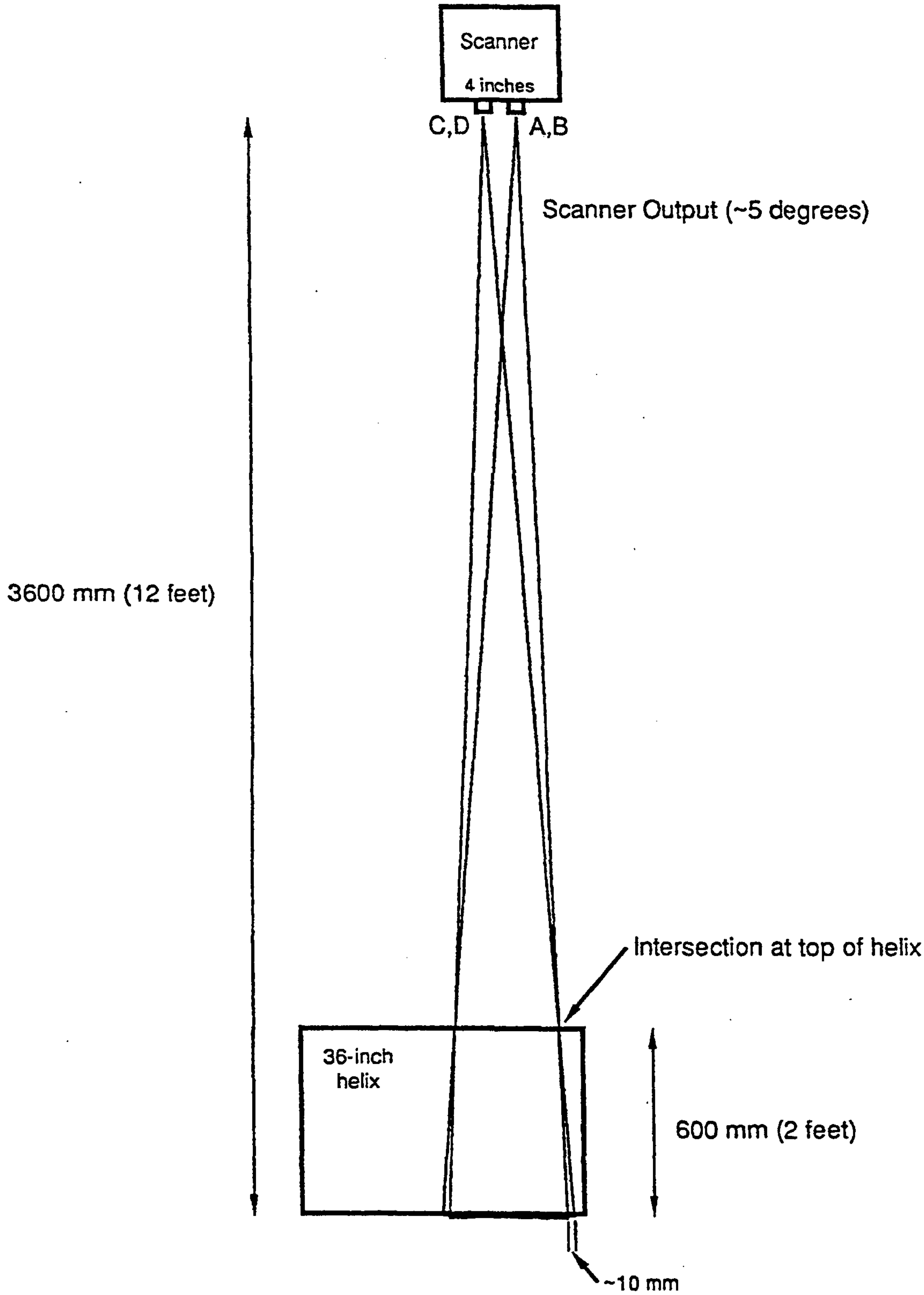


Figure 1-25. Scale drawing of convergence on 36-inch helix with no folding mirrors.

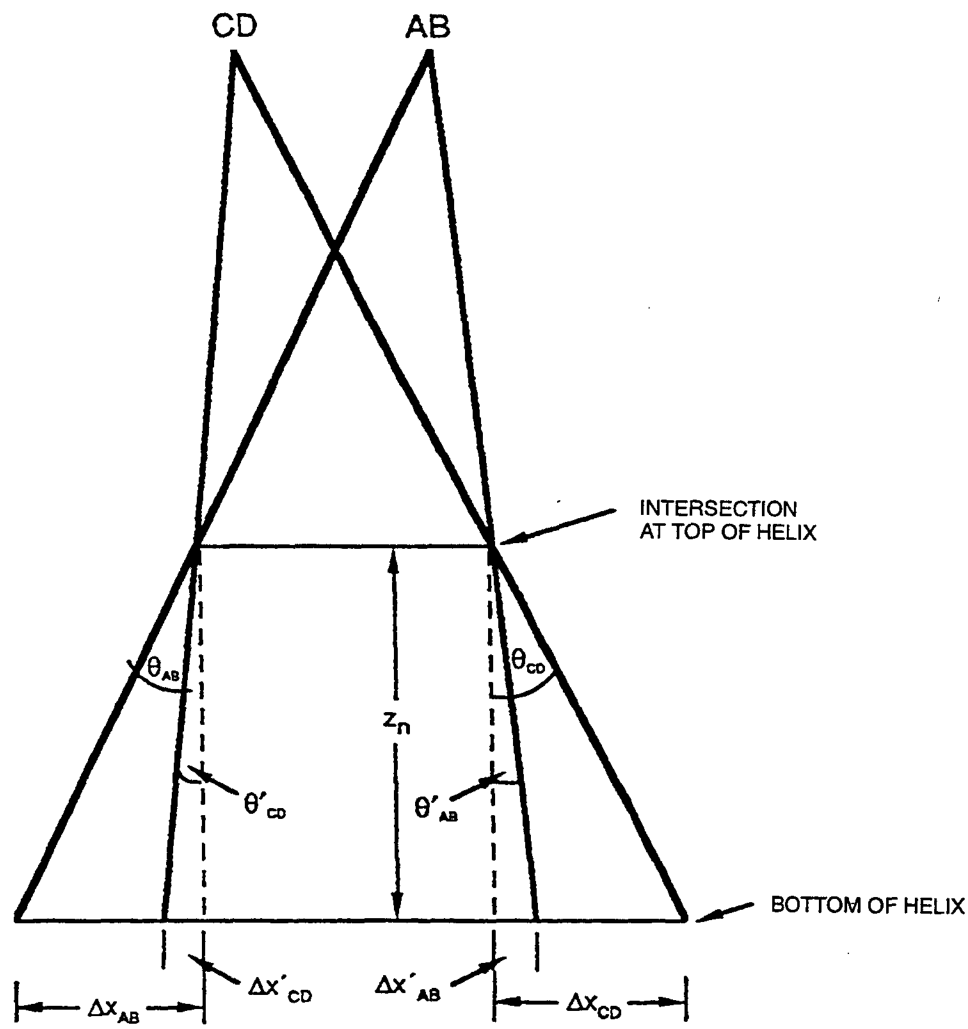
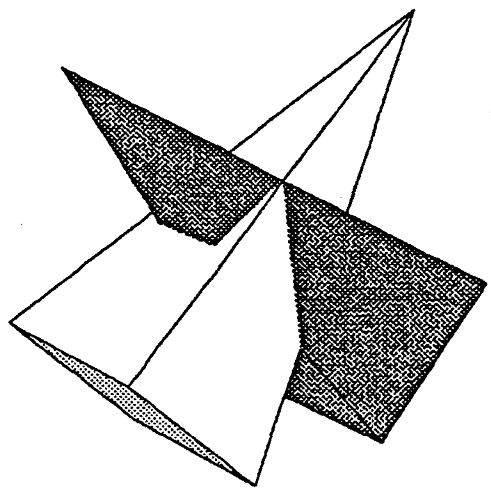
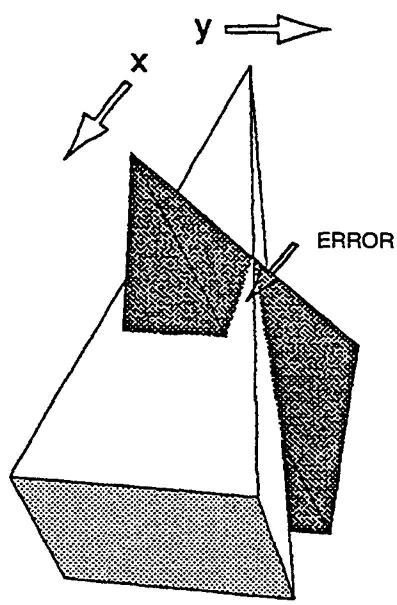


Figure 1-26. Exaggerated view of helix convergence showing relevant parameters.

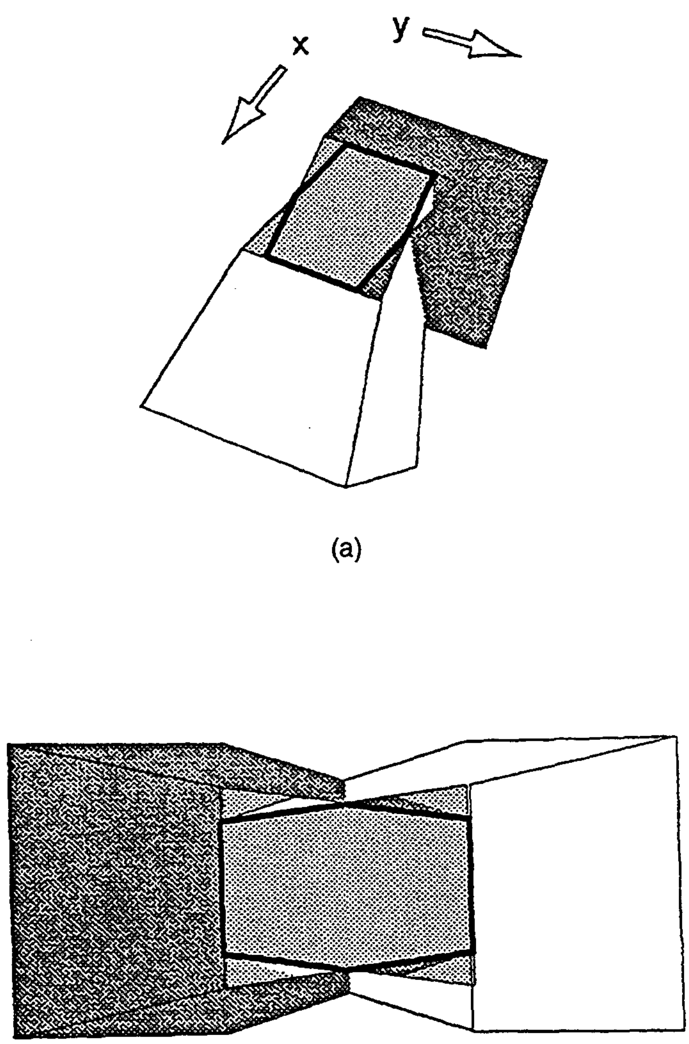


(a)



(b)

Figure 1-27. Exaggerated 3-D view of the two "pyramidal" scans coming from channels A and B and C and D of the four-channel scanner showing the mismatch in the y-axis direction.



(a)

(b)

Figure 1-28. Exaggerated 3-D view of the two "pyramidal" scans coming from channels A and B and C and D of the four-channel scanner showing a slice through the intersection plane at the top of the helix.

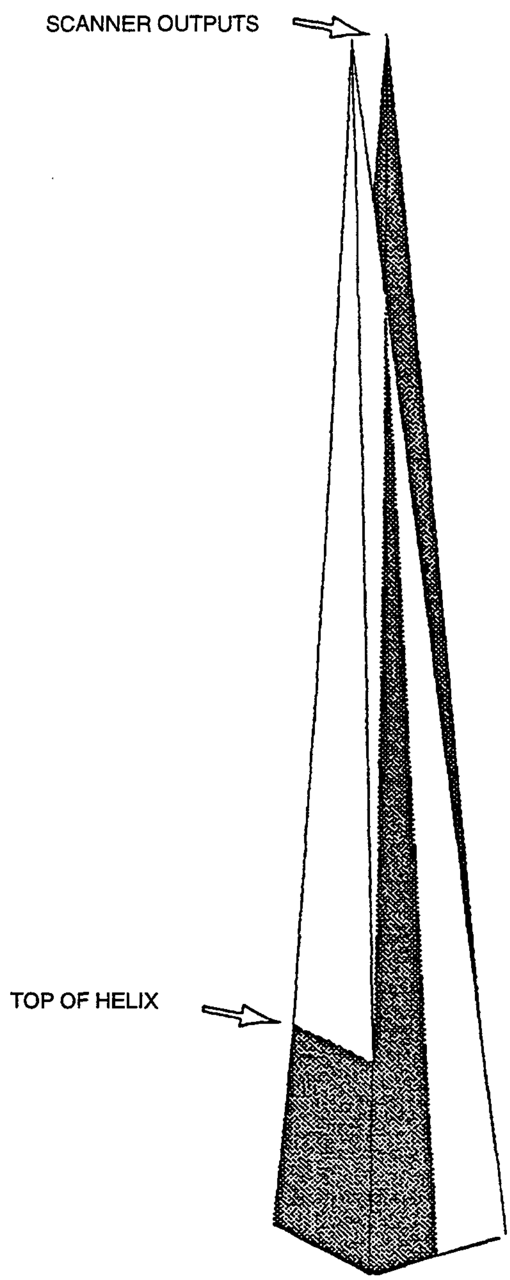


Figure 1-29. Scale drawing of 3-D view of the two “pyramidal” scans coming from channels A and B and C and D of the four-channel scanner (folding mirrors removed).

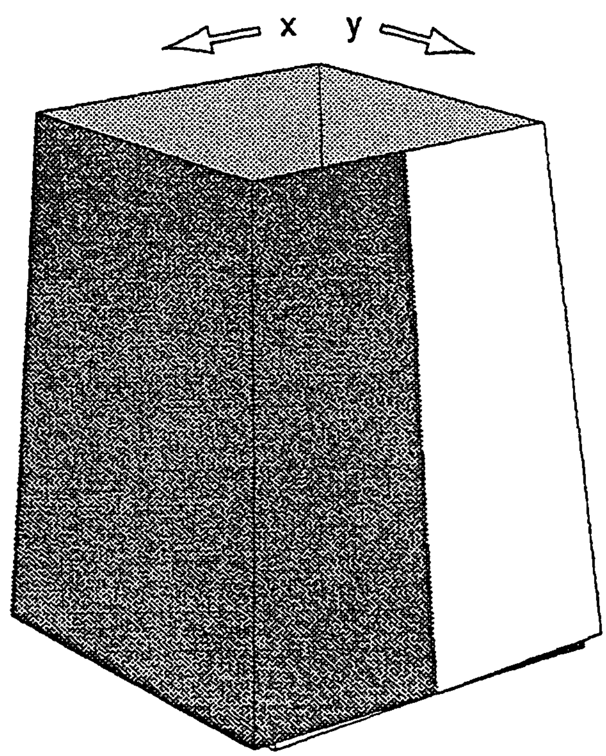
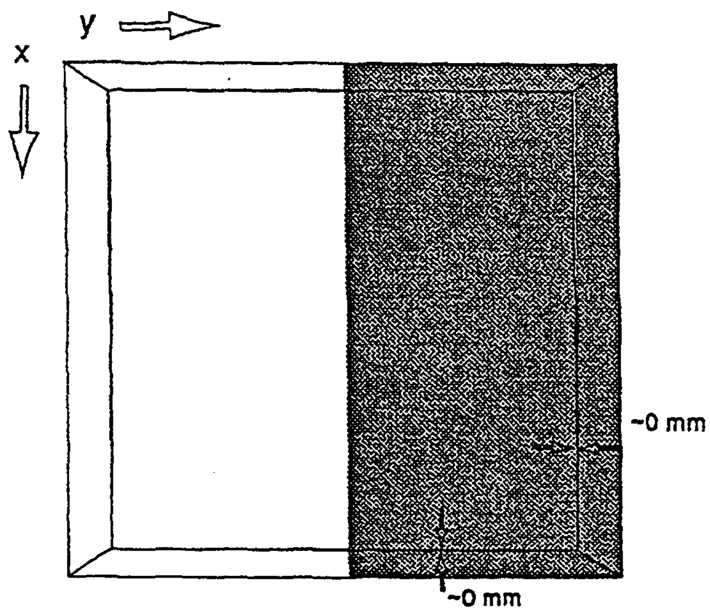
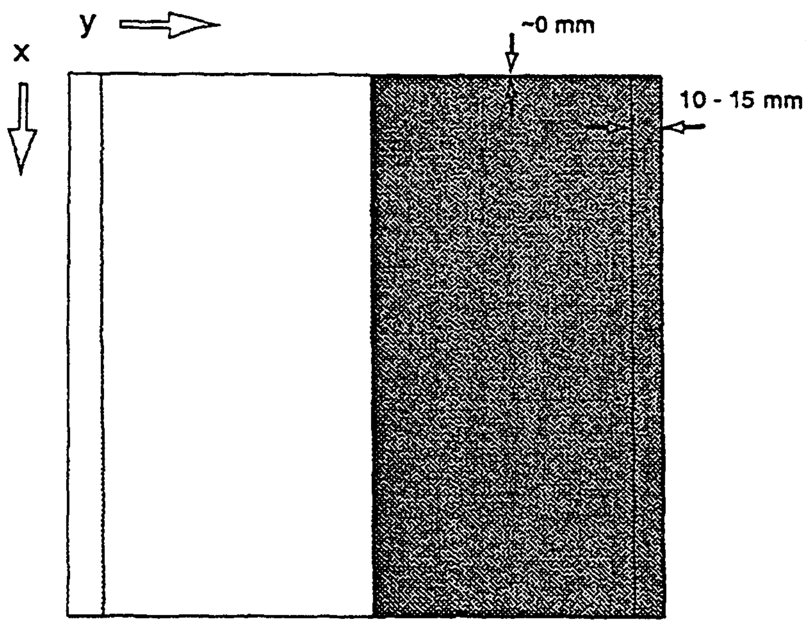


Figure 1-30. Scale 3-D view of the two "pyramidal" scans coming from channels A and B and C and D of the four-channel scanner showing section from top to bottom of helix.



(a) INTERSECTION AT TOP OF HELIX



(b) INTERSECTION AT BOTTOM OF HELIX

Figure 1-31. Intersection of two-beam scan at top and bottom of helix from figure 1-30.

Color convergence is also an issue that must be addressed eventually. Because acousto-optic beam deflection is proportional to the optical wavelength, the red scanner will have a wider scan angle than the green, which, in turn, has a wider scan than the blue. We do not want to correct for this by using only software as this would produce less resolution in red than in the blue. Telephoto projection lenses are needed to adjust the angular magnification over a continuous range to achieve rough alignment. Then, software can make the necessary minor corrections.

6. FOUR-QUADRANT VOLUMETRIC DISPLAY SYSTEM

The volumetric display system previously described shows a projected image in only one quadrant of the helix volume. While this has proven useful for several years, it does not make full use of the entire helix volume. In 1997, a new design was implemented that distributes the four channels of the existing red and green scanners into the four quadrants of the helix. Thus, each quadrant has up to 10,000 green voxels and 10,000 red voxels. Currently, the single-channel blue scanner projects 10,000 voxels into one quadrant.

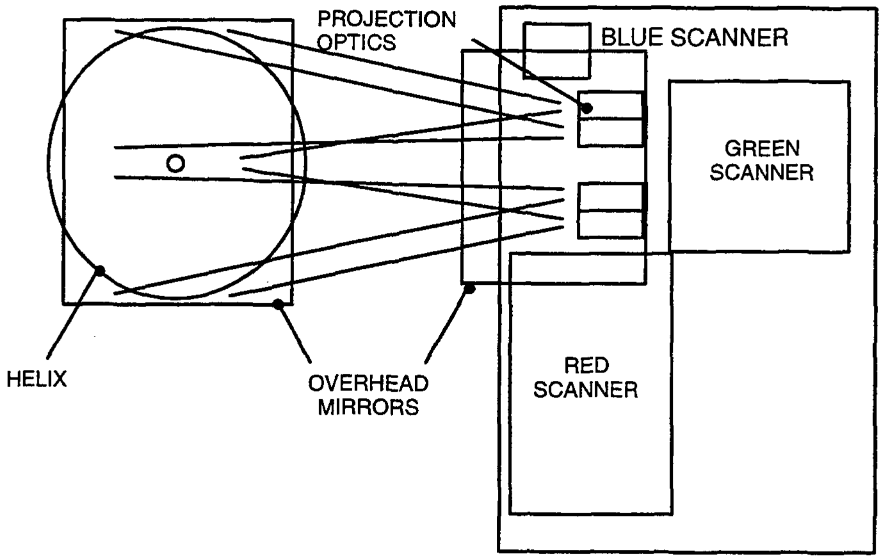
To achieve four-quadrant operation, the scanner projection optics were redesigned. A diagram of the optical layout is shown in figure 1-32. A major achievement was the incorporation of the latest commercial laser technology, diode-pumped Nd:YAG lasers (CASIX Model DP110). These were used to replace the argon ion laser for the green output. Fortunately, the wavelength change from 514 to 532 nm did not impact the acousto-optic scanner design in any major way. Two lasers of 100 mW each were used, one for Channels A and B, the other for Channels C and D. For the red scanner, the krypton ion laser was replaced with four standard helium-neon lasers (Melles Griot Model 05-LHP-925, 20 mW), one for each channel. The superior efficiency of the red scanner allows the use of low-power lasers. Both red and green lasers are free of any water cooling requirements and use about 1,000 times less electrical power. Currently, the blue scanner uses an argon ion laser, but solid-state blue lasers are now commercially available. In addition, these lasers allow the design of truly transportable volumetric display systems. The next section covers such a design. (See figure 1-33.)

The overhead folding mirrors were increased in size to accommodate the expansion of the projection system. Standard dichroic mirrors were used to combine the red, green, and blue channels. The projection optics consist of a series of three lenses. The first (300-mm) and third (120-mm) lenses provide the rough overall expansion and focusing of the scan. The second lens (200-mm) acts as a fine adjustment for expanding or contracting the image size.

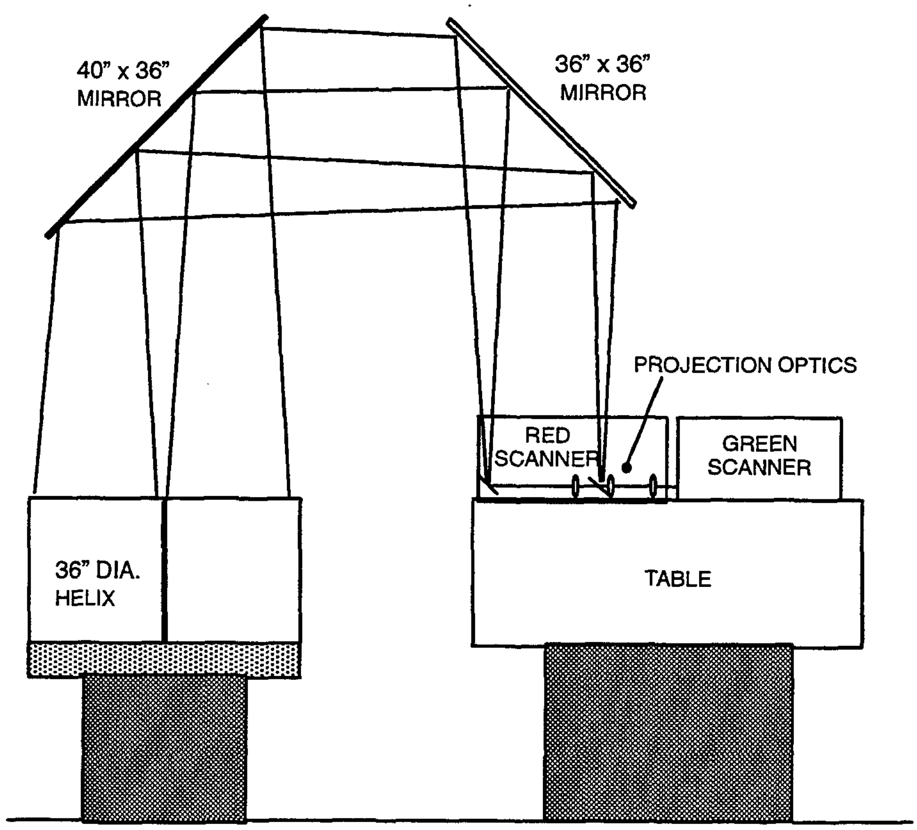
The performance of this system is basically the same as the older single quadrant system described previously, except that now there are no restrictions as to where voxels can be placed (excluding the center shaft). The viewability of the display is greatly improved, as well as making more efficient use of the helix volume.

7. SYSTEM TRADE-OFF ANALYSIS

A specification spreadsheet was developed as a design aid in determining system parameters for various hypothetical 3-D helix systems. The total number of voxels, helix size, scanner type and resolution, voxel radiance, laser and power requirements, etc. are covered in table 1-3. The equations below the table are based on the timing considerations typically used in the current generation of laser scanners and interface electronics.



TOP VIEW



SIDE VIEW

Figure 1-32. Top and side views of the second-generation four-quadrant 3-D Volumetric Display System.

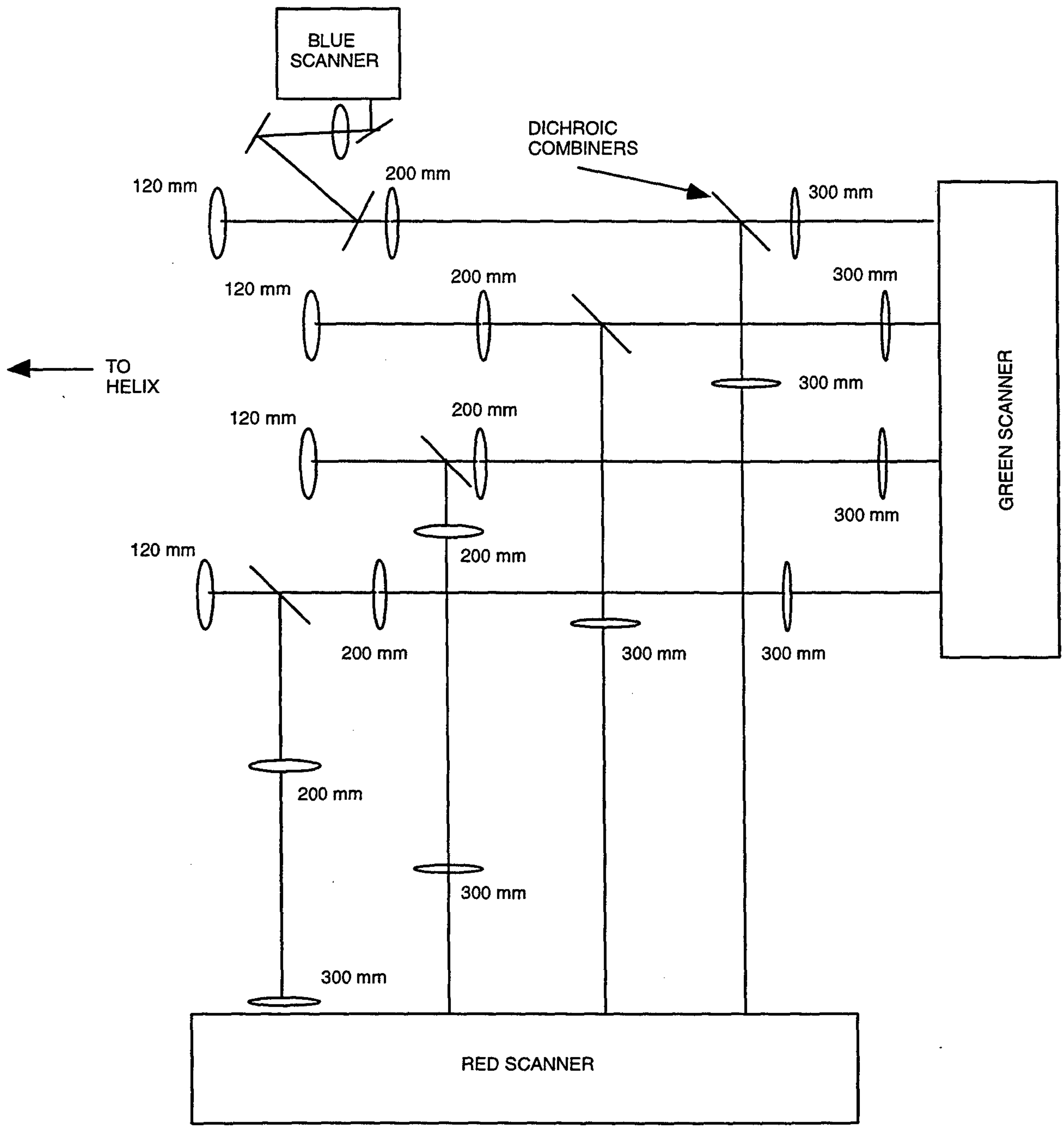


Figure 1-33. Detailed view of four-quadrant projection optics showing lens layout.

Table 1-3. 3-D Volumetric Display System specification.

System	Voxels	Resolution	Helix Size	Display Area	Scanner Type	Scanner Efficiency	τ (usec)	Pv/Pin 1.00E-06	Vox. Radiance mW/cm2	Lasers R / G / B	Water?
1	40,000	400	36"	12"x12"	200 MHz 4-ch.	0.03	2	0.45	0.08	Kr/YAG/Ar	yes
2a	10,163	256	20"	7"x7"	50 MHz	0.11	4.92	10.82	2.24	Kr/YAG/Ar	no
2b	4,340	512	20"	7"x7"	"Pockels"	0.11	11.52	25.34	21.02	Kr/YAG/Ar	no
3	25,000	250	20"	7"x7"	125MHz "Pockels"	0.03	2	1.20	0.24	Kr/YAG/Ar	no
4a	10,000	256	20"	7"x7"	NEOS 4-ch.	0.13	4.92	9.80	2.03	Kr/YAG/Ar	no
4b	20,000	256	20"	7"x7"	NEOS 4-ch.	0.13	4.92	3.30	0.68	Kr/YAG/Ar	no
4c	30,000	256	20"	7"x7"	NEOS 4-ch.	0.13	4.92	1.14	0.24	Kr/YAG/Ar	yes
4d	40,000	256	20"	7"x7"	NEOS 4-ch.	0.13	4.92	0.05	0.01	Kr/YAG/Ar	yes
5	40,000	256	20"	7"x7"	NEOS 4-ch.	0.13	4.92	0.05	0.01	YAG (4)	no
6	40,000	256	36"	12"x12"	NEOS 4-ch.	0.13	4.92	0.05	0.004	Ar	yes
7	4,096	512	13"	4"x4"	NEOS 1-ch.	0.13	11.52	1.79	4.54	Kr	yes
8a	20,000	400	20"	7"x7"	200Mhz 4ch	0.04	2	1.60	0.81	red diode	no
8b	4,340	512	20"	7"x7"	"Pockels"	0.18	11.52	41.48	34.40	red diode	no
8c	4,096	512	20"	7"x7"	NEOS 1-ch.	0.2	11.52	2.75	2.28	red diode	no

$$\frac{P_v}{P_{in}} = \frac{\eta}{T_r}\left(\frac{cT_r}{V_{max}} - \tau\right)$$

Tr = 20 Hz refresh period.
Pv is the average voxel power.
Pin is the total laser power
(must + 4 for 4-ch. system).

For a "Pockels" Scanner: $V_{max} = \frac{cT_r}{2\tau}$ *and* $\frac{P_v}{P_{in}} = \frac{\eta}{T_r}(\tau)$

c = number of channels.
τ = access time.
η = scanner efficiency (per channel).
Vmax = total number of voxels in the system.
Voxel radiance is referenced to Pin = 1 Watt.

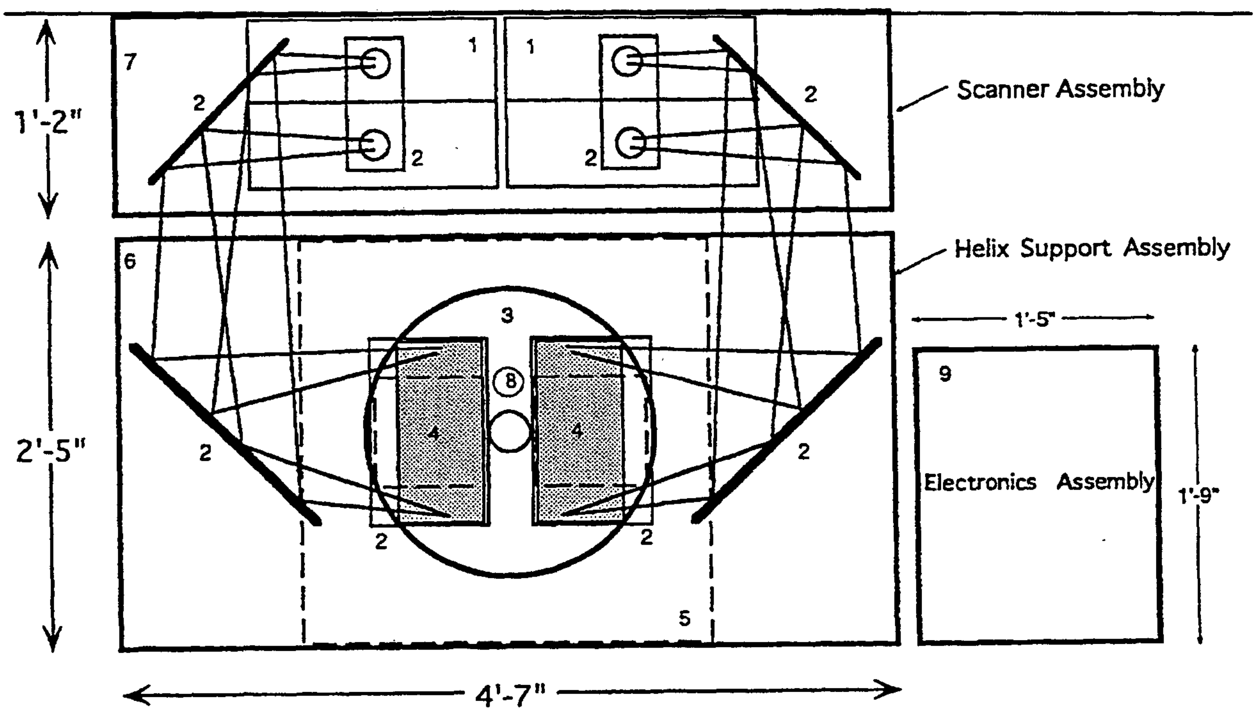
Tr = 0.05

Table 1-3. 3-D Volumetric Display System specification (Continued).

System	Optical Power(mW) for 100 nW voxel	System Electrical Power	Advantages	Disadvantages	Cost
		Lasers / Electronics			Lasers / Scanners / Misc
1	222	14 kW / 650 W	Large display, high res. many voxels	water-cooled lasers, Cost, poor eff. unproven design, big footprint	$60 K / $200 K / $100 K
2a	9	9 kW / 500 W	high eff., no water	low # of voxels, unproven design	$40 K / $90 K / $100 K
2b	4	9 kW / 500 W	bright voxels,high eff., high res. high reolution, no wasted light	low # of voxels, unproven design	$40 K / $90 K / $100 K
3	83	9 kW / 500 W	many voxels, no water no wasted light	unproven scanner, low eff.	$60 K / $150 K / $100 K
4a	10	4 kW / 650 W	bright voxels, no water	low number of voxels	$40 K / $120 K / $100 K
4b	30	4 kW / 650 W			$60 K / $120 K / $100 K
4c	88	8 kW / 650 W			$60 K / $120 K / $100 K
4d	1923	14 kW / 650 W	many voxels	water-cooled lasers, Cost, poor eff. big footprint	$60 K / $120 K / $100 K
5	1923	2 kW / 650 W	low power consumption, small size many voxels	monochrome, 4 YAGs required	$60 K / $40 K / $100 K
6	1923	7 kW / 650 W	many voxels, large display	monochrome, water-cooded laser	$60 K / $40 K / $100 K
7	56	4 kW / 650 W	bright voxels	monochrome, water-cooled low voxels	$60 K / $40 K / $100 K
8a	62	20 W / 650 W	low power, compact, many voxels	monochrome	$60 K / $40 K / $100 K
8b	2	10 W / 500 W	low power, bright voxels, compact	monochrome	$60 K / $40 K / $100 K
8c	36	10 W / 350 W	low power consumption, compact	monochrome	$60 K / $40 K / $100 K

8. DESIGN OF TRANSPORTABLE 3-D VOLUMETRIC DISPLAY

A great deal of interest has been generated by the 13-inch and 36-inch laboratory-based systems. Many potential users of the 3-D helix volumetric display have expressed the desire for a more compact system. The goal was to have a system that required less volume and power requirements while maintaining a useful number of voxels and having some color capability. After many iterations, such a design was developed consisting of a two-color (red/green) system. The total voxel count is 160,000 (80,000 per color). Figure 1-34 is a top view of the system showing the three basic assemblies: the scanner assembly, the helix support assembly, and the electronics assembly. The scanner assembly consists of four red-green scanner subassemblies, each capable of 20,000 voxels per color (figure 1-35). Two of these scanner modules display on one-half of the helix, while the other two modules display on the other half. The helix for this system was chosen to be translucent to enable illumination from below. An extensive materials evaluation program was undertaken to find the most suitable plastic host and diffusing material for the helix. Figure 1-36 shows a side view of the system. The scanner and helix support assemblies are shown split apart for clarity. The lasers for this system, two 250-mW diode-pumped, doubled Nd:YAG+s for the green and eight single-mode red diode lasers. Table 1-5 shows a list of specifications for the system. Figure 1-37 shows a pictorial view of how the two display volumes are situated in the translucent helix/cylindrical housing.



2-Color, 2-Image System
80,000 vox/color, 160,000 total
Top View of Table

1 Laser Scanner Module
2 Mirror
3 24-inch Translucent Helix
4 Display Area
5 Support Base for Helix
6 Helix Enclosure
7 Scanner Enclosure
8 Motor
9 Electronics

Figure 1-34. 3-D Volumetric Display System—transportable model, top view.

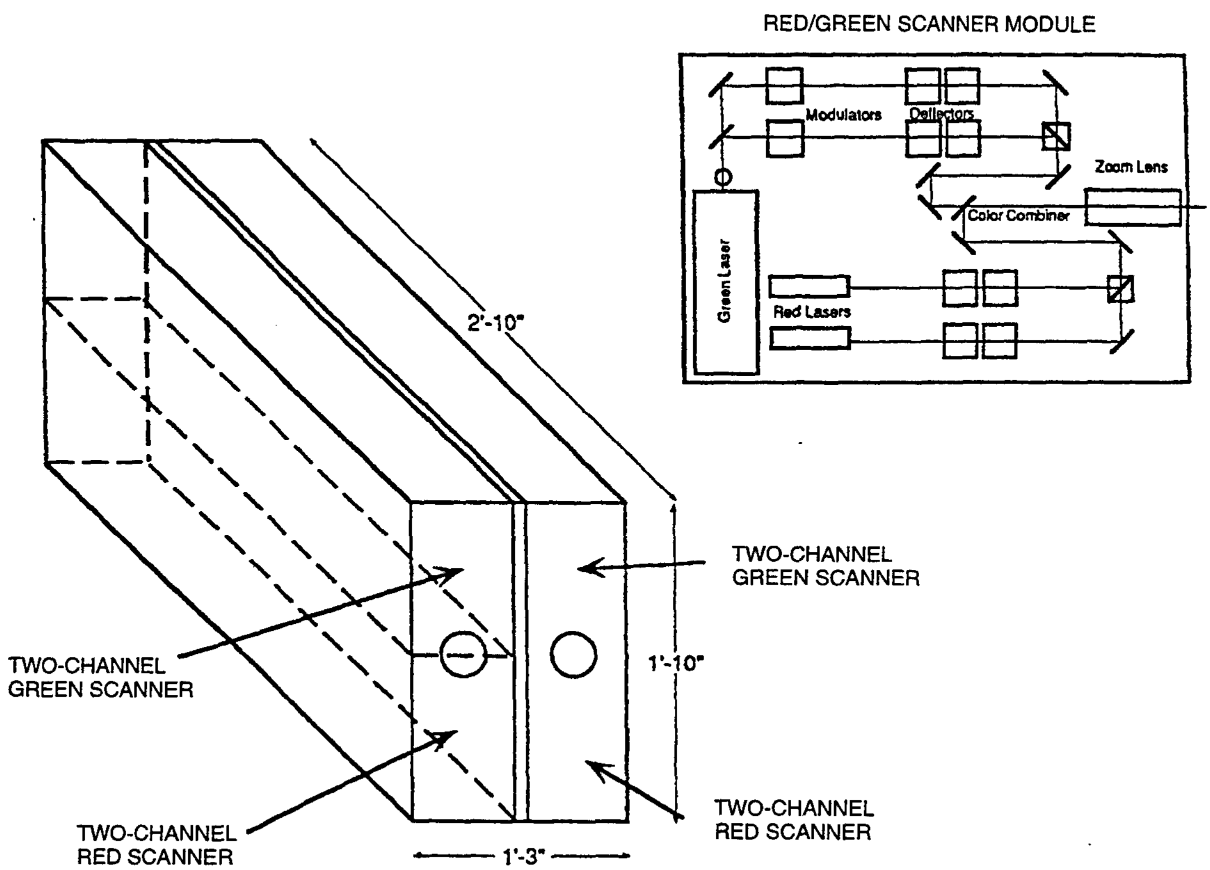
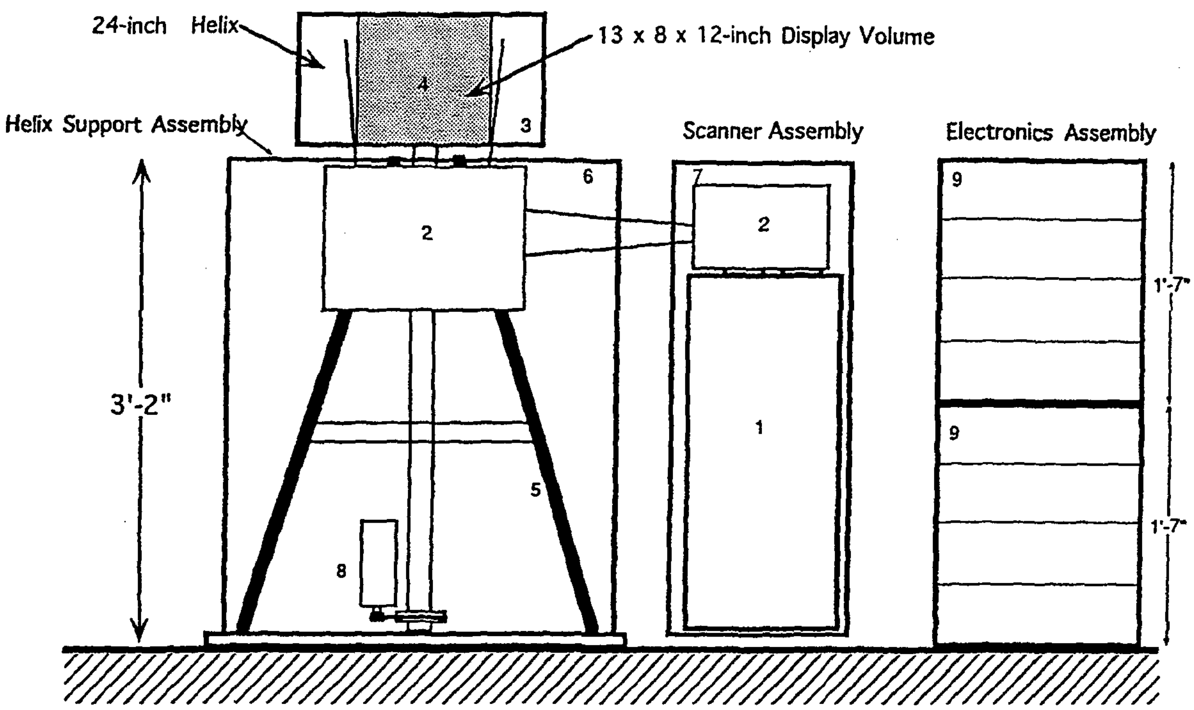


Figure 1-35. Proposed design for a two-color, eight-channel laser scanner.



2-Color, 2-Image System
80,000 vox/color, 160,000 total
Side View of Table

1 Laser Scanner Module
2 Mirror
3 24-inch Translucent Helix
4 Display Volume
5 Support Base for Helix
6 Helix Enclosure
7 Scanner Enclosure
8 Motor
9 Electronics

Figure 1-36. 3-D Volumetric Display System—transportable model, side view.

Table 1-4. Transportable volumetric helix display—system specifications.

Item	Characteristic
Display Surface	Axially Symmetric Translucent Double Helix
Rotational Axis	Vertical
Rotation Rate	600 RPM
Display Volume	20,000 cm^3
Volume Dimensions d = cylinder diameter h = height D = dead zone diameter	 d = 61 cm h = 30 cm D = 6 cm
Illumination Method	Passive Translucent Screen with Scanned Laser Beams Projected from Bottom
Scanning Method	Acousto-Optic
Voxel Size	1.5 mm
Voxel Refresh Per Rotation	2
Frame Rate	20 Hz
Vodel Addressing in XYZ	4096 × 4096 40,000 per color per display volume totaling 160,000 voxels
Number of Colors	Red, Green, Yellow, Orange
Maximum Voxels Per Frame	Area 1 = 80 K voxels/frame × 20 frames = 1.6 million voxels/sec Area 2 = 80 K voxels/frame × 20 frames = 1.6 million voxels/sec Total = 3.2 million voxels/sec
Laser Power and Cooling Requirements	Thermo-electric cooling of two 250 mW green NdYAG, eight 30 mW red diode lasers
Laser Safety	20 mW per image (average) (Less than 15 mW Industrial Safety Limit)
Illuminance (Brightness)	Approximately 1 ft-Lambert or User Specified

From this design exercise, a transportable Volumetric Display System was developed by the SSC San Diego engineering team. In applications where size is a major constraint, such as shipboard or submarine displays, a 36-inch 3-D display may not be desirable. To make the system as compact as possible, the helix surface material was changed to a translucent material (20 mil polystyrene) to allow laser projection to come from below the helix. Also, the helix diameter was reduced to 12 inches, which allows a much shorter projection distance from the laser scanners. The polystyrene helix was vacuum-formed over a mold and then secured by suspending from a thin frame. A stationary, clear acrylic cylindrical housing acts as a safety enclosure. Figure 1-38 shows a drawing of SSC San Diego's first transportable display system.

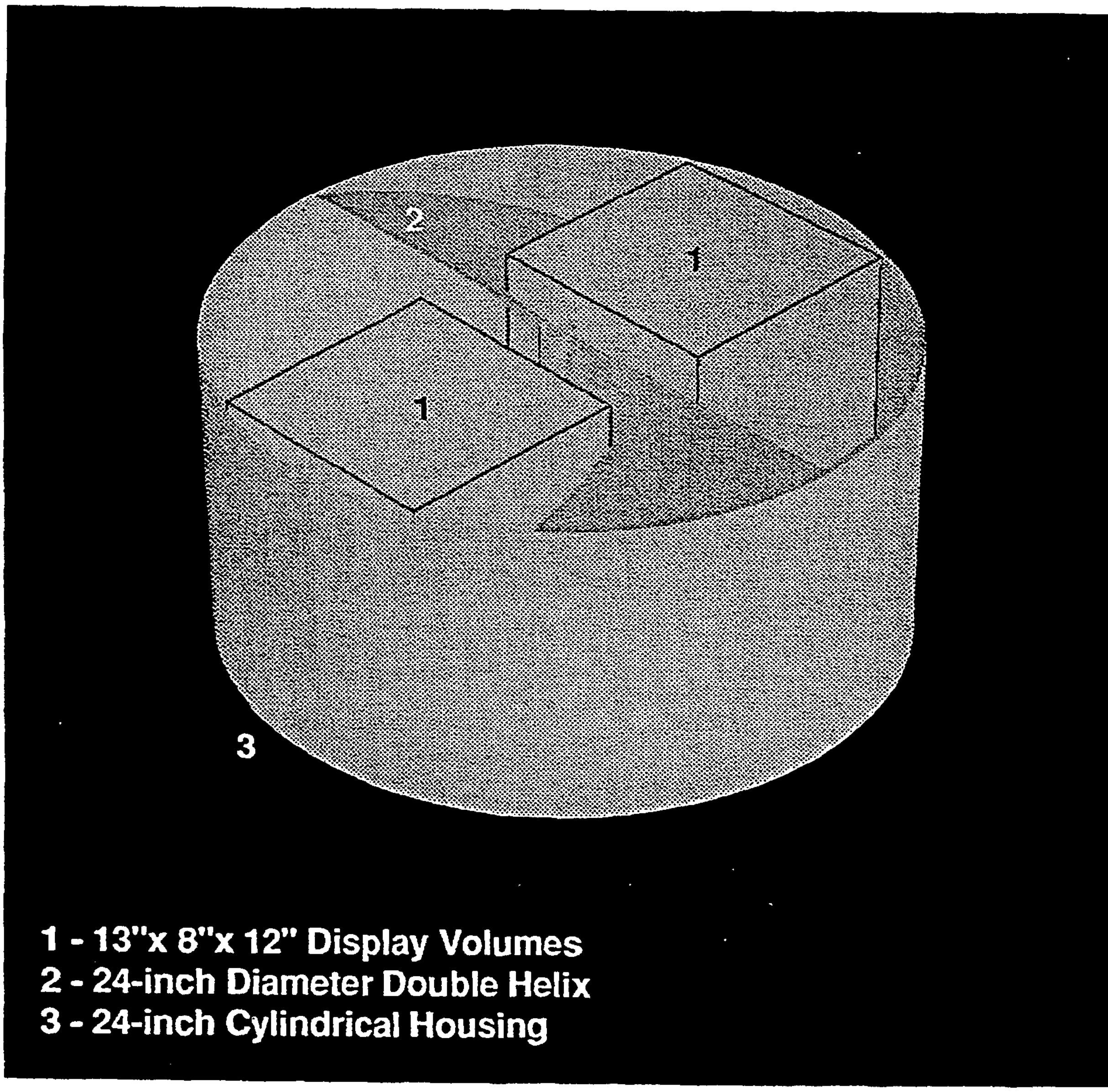


Figure 1-37. 3-D Volumetric Display System—transportable model, translucent helix.

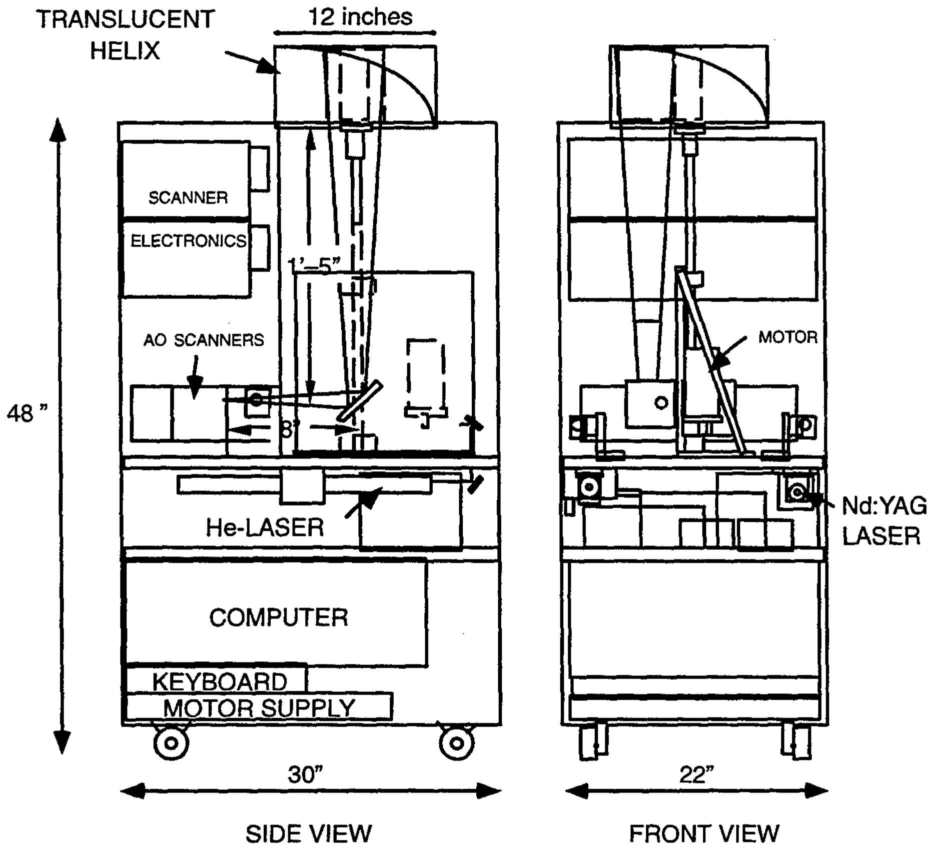


Figure 1-38. 12-inch diameter, helix-based, two-color, transportable 3-D Volumetric Display System.

The AO scanners used for this system produce 4,000 voxel images at a 20-Hz refresh rate. They are similar in design to one channel of the scanners used on the 36-inch system. Two such scanners were used, one for red using a 20-mW HeNe laser (633 nm), and one for green using a 100-mW doubled diode-pumped Nd:YAG laser (532 nm). The voxel size is 0.7 mm. The interface electronics and programming schemes used were similar to those on the larger system described earlier.

One of the disadvantages of the 36-inch reflective helix is the appearance of occlusion zones when one of the helix blades blocks a portion of the displayed image. The main advantage to the translucent helix is the improved viewing angle around the display created by projecting the laser beams from below. Measurements made of the occlusion zones of this system show a significant increase in viewability over the reflective helix. In addition, it was found that a further increase could be obtained by removing one blade of the double helix surface, yielding an over 300-degree viewing zone. Improvements in more precise mold fabrication and better 50/50 transmission/reflection characteristics should further increase the viewability range of the display.

9. TRANSFER OF 3-D VOLUMETRIC DISPLAY TECHNOLOGY TO INDUSTRY

Many lessons were learned while taking SSC San Diego's transportable system on the road to several conventions. Improvements in ruggedization, laser power, more voxels, and expansion to four quadrants were needed. In 1995, a Cooperative Research and Development Agreement (CRADA) was signed with NEOS Technologies, Inc. and RGB Technology, Inc. to develop a commercialized version of the volumetric display that incorporated these changes. The goal was to produce a system that was transportable and reasonably affordable for both military and government applications. The first such system was deployed on the USS *Stennis* for the Joint Warrior Interoperability Demonstration (JWID 97) where it was interfaced to a LINK 16 tactical data feed. After further improvements this system was finally delivered to SPAWAR for installation into the Command Center of the Future. Figure 1-39 shows a picture of the system. It uses a single spiral translucent helix, with red and green solid-state laser scanners for each quadrant. Because of the single helical spiral, the surface spins at 1200 rpm to produce a 20-Hz refresh rate. The system produces up to 20,000 of red and green per quadrant per frame for a total of 80,000 voxels per frame, or 80,000 x 20 = 1.6 million voxels per second.

Figure 1-39. Transportable 3-D System developed by NEOS/RGB for SSC San Diego's Command Center of the Future.

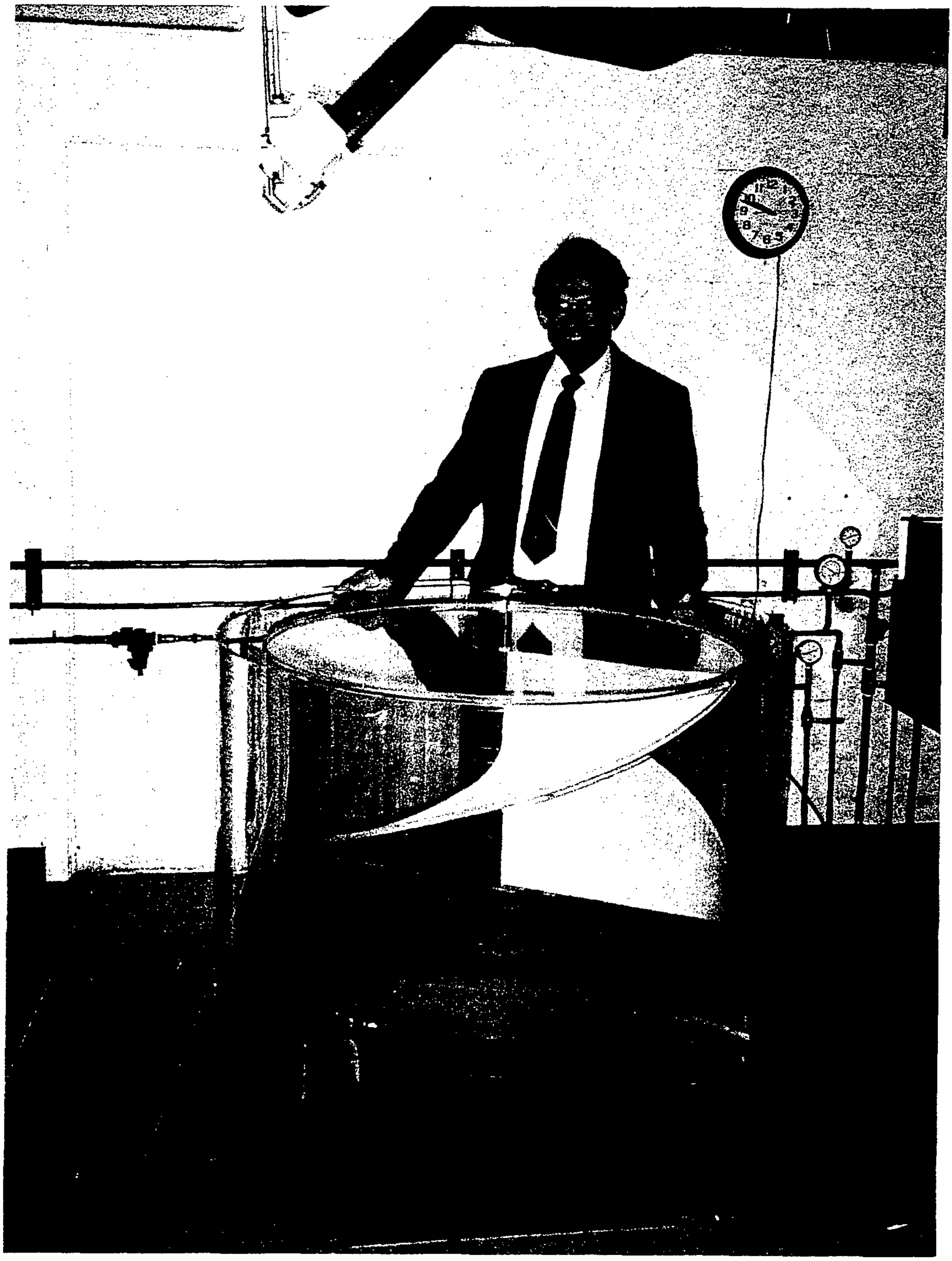
10. SUMMARY

The FY 93 3-D Volumetric Display Team was successful in building a 36-inch diameter display system capable of producing 40,000 voxels per frame at a 20-Hz refresh rate (800,000 voxels per second). The main accomplishments were the improved noise reduction in the helix, an order-of-magnitude increase in the number of voxels displayed (40,000 vs. 4,000), and improved electronic control cards. The improved performance in the AO scanners was achieved by parallel combination of four 10,000 voxel scanners and four independent AO modulators. Analysis of the modulators provided insights enabling improvements in the beam quality at the helix, producing a more circular spot with minimized diffraction effects. By optimizing the scanner addressability and resolution, the spot size was reduced from 5 mm to 2 mm. A general design method was devised to study the various system trade-offs and as an aid to future system analysis. The spot size, brightness, and required scanner and projection optics can all be analyzed once a set of system parameters has been determined (number of voxels, desired resolution, helix diameter, laser source, scanner type, etc.). Using this analysis, a major upgrade effort was conducted in 1997 to illuminate all four quadrants of the helical volume. A redesign of the projection optics now allows up to 10,000 voxels to be displayed per quadrant, per color. Solid-state lasers have now replaced the large, water-cooled, inefficient krypton and argon ion lasers, greatly improving the practicality of transportable system development.

A preliminary design was carried out for a transportable system that could be taken apart and shipped in three or four containers. It uses a 24-inch-diameter, translucent helix, and a more compact design to achieve a two-color (red, green), 160,000 total voxels per frame, 20-Hz refresh system. The high voxel count is obtained by using two separate volumes, one on each half of the helix. From this study, a transportable volumetric display system was constructed in a standard rack enclosure using two scanners, one for red and green, projecting from underneath a 12-inch translucent double helix. The unit was sent across the country and displayed at several conventions

The success of SSC San Diego's prototype transportable display generated a great deal of interest, showing potential for marketing a commercial version. In 1995, a Cooperative Research and Development Agreement (CRADA) was signed to initiate the transfer of 3-D Volumetric Display technology to industry. A partnership between SSC San Diego, NEOS Technologies, Inc., and RGB Technology, Inc. produced the first commercially available, transportable 3-D volumetric display. The system was first deployed onboard the USS *Stennis* as part of the JWID 97 demonstration. After further refinements, the system was installed in SSC San Diego's Command Center of the Future, giving the commander a global perspective and increasing the situational awareness of tactical situations.

SECTION 2. 3-D MOVING CHAMBER (HELIX)



Malvyn McDonald, Helix and Mechanical Design Lead Engineer.

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SECTION 2. 3-D MOVING CHAMBER (HELIX)

1. INTRODUCTION

The 3-D Volumetric Display System allows true three-dimensional visualization of computer-generated images. A beam from the system's laser, guided by an acousto-optic (AO) scanner, is projected through a volumetric display medium. The display medium allows the laser beam to create discrete visible dots of light called "voxels" at any point within its imaging volume. Arrays of voxels are used to create images that are perceived by an observer from a perspective relative to his/her position.

1.1. HELICAL DISPLAY SYSTEM

The Volumetric Display System developed at Space and Naval Warfare (SPAWAR) Systems Center, San Diego (SSC San Diego) is comprised of three major subsystems: 1) a laser optics system; 2) a computer-based controller; and 3) a helical display assembly. The laser optics system creates, modulates, and guides laser signals and projects them through a display medium. The computer-based controller processes instructions and other data and generates the electronic modulation and deflection signals that regulate the laser scanner and converts the beam into imaging pulses. The helical display is a volumetric medium that uses simple optical and mechanical principles to transform the scanned laser pulses into visible three-dimensional images.

A primary element in the helical display system is a rotating helically curved screen, referred to as the "helix." Figure 2-1 illustrates its operation. A short-duration laser pulse striking the screen is diffused, creating a momentary visible spot or voxel at the point in space where they intersect. Images

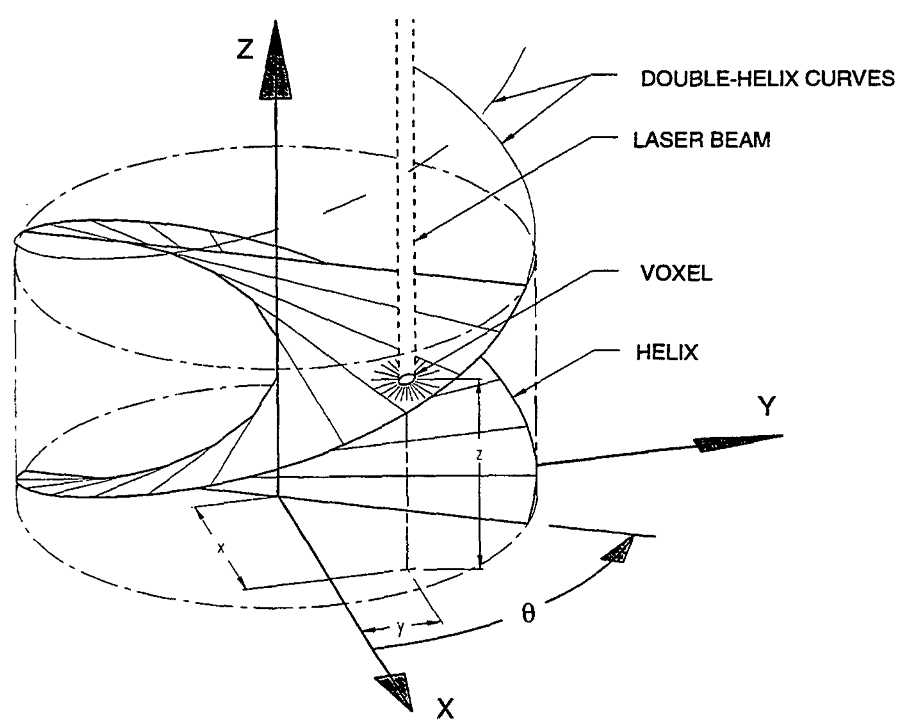

Figure 2-1. Helical display operating principles.

created by arrays of voxels can be generated anywhere within the volume swept by the helix. The light-scattering characteristics of the screen make the images visible to all observers within a large viewing angle. The shape of the helical screen may be described as a spiraling surface extended between the two curves of a diametrically opposed double-helix. Its cross section in any plane perpendicular to the axis of the double-helix is a straight line through the axis. The surface is bounded at the top and bottom so that its overall height represents 180 degrees of rotation of the vertical double-helix. The configuration of this surface allows its interaction with a vertical laser beam to be easily expressed in simple mathematical terms. Referring to the Cartesian coordinate system in figure 2-1, any planar position (x, y) assumed by the vertical laser beam in concert with any angle of rotation, Θ, of the helix is sufficient to predetermine the vertical position, z, of the resulting voxel. The three-dimensional location of a voxel may, thus, be controlled by manipulating only the planar position of the beam and rotational angle, Θ, of the helix. By synchronizing the release of each laser pulse with the appropriate angle of a constantly rotating helix, the simple transformation of an array of x- and y-scanned laser pulses into a assemblage of voxels is achieved, creating a three-dimensional image. The helical shape possesses the novel characteristic of allowing voxels to be created anywhere within the volume, bounded by its overall height and diameter.

Placement of the voxels is directed by an AO scanner and controlled by a computer-based electronic driver card. Planar placement (x, y coordinates) of the vertical laser beam is regulated by AO beam deflectors within the scanner. The beam is folded by a system of mirrors that increases its length sufficiently to amplify the small angular variations at the deflectors into large lateral deflections and place it in a vertical attitude. The scanner also contains AO modulators that regulate the timing and duration of each laser pulse, thus controlling vertical placement (z coordinate) of each voxel. Input data to the modulator drivers is generated by a central processor, using angular position and rotational speed data gathered by an encoder directly from the helix.

1.2. FIRST-GENERATION LABORATORY DISPLAY

Several laboratory models of the helix have been fabricated to demonstrate the feasibility of the system and to explore its potential applications. The first-generation models were machined from solid aluminum billets. The largest of these, 13 inches in diameter and 5 inches high, was designed to demonstrate the most prolific scanner available at that time, having the capability of generating 4,000 voxels, 20 times per second. Because this model is opaque, it must be projected on and viewed from the same side. It is mounted with its spin axis in a horizontal attitude to facilitate this effect. To enhance reflectance and light diffusion characteristics, the model's display surface is treated with an opaque white finish. It is axially driven by a 1/2-horsepower DC motor and fitted with a Hall-effect position-sensing unit.

The helical screen is axisymmetric about its spin axis so that it sweeps through the cylindrical display volume two times per revolution. At a design speed of 600 rpm, images are refreshed 20 times per second. At this rate, the visual effect known as "flicker" effectively disappears and animated motion appears continuous.

The arrangement of the laser optics is shown schematically in figure 2-2. It consists of an argon/krypton white light laser, a dispersing prism to separate its colors, masking shutters, mirrors, and lenses that collimate the laser beam, two AO modulators and AO scanners, and beam projection optics. The first-generation system displays images in red or green in separate quadrants of the 13-inch display volume.

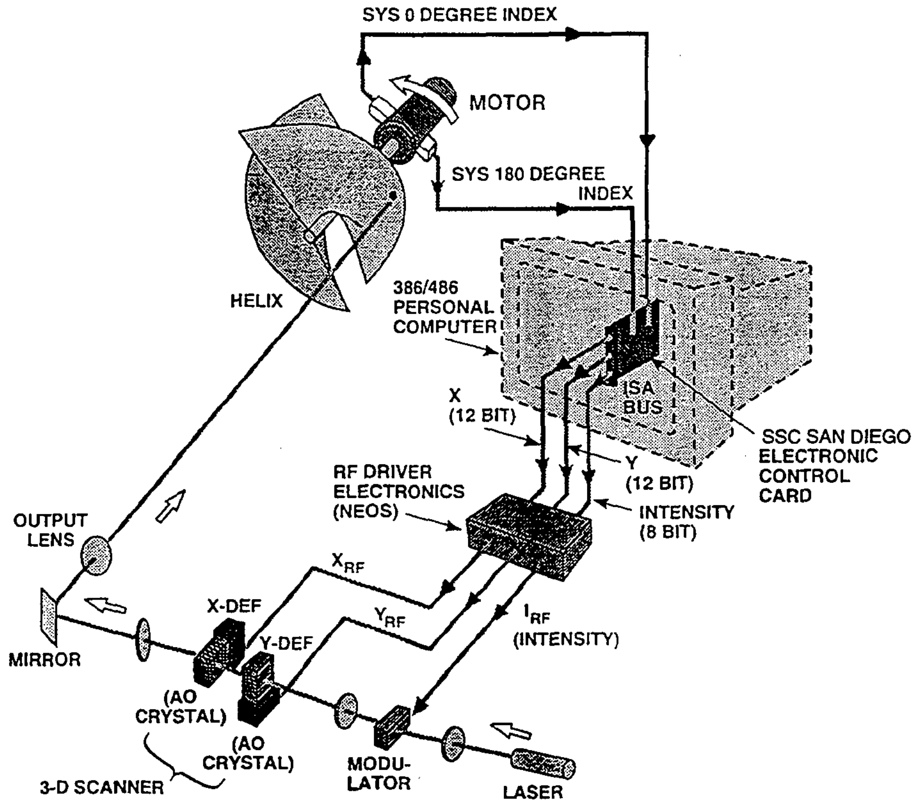

Figure 2-2. 3-D Volumetric Display laser optics arrangement.

The SSC San Diego-designed interface control card, Volumetric Display Refresh Generator #1 (VDRG1), allows the display of 4,200 voxels per color at a refresh rate of 20 Hz. Display and control data are processed by an IBM PC-compatible computer.

1.3. SECOND-GENERATION DISPLAY

In the second-generation AO scanner, designed and built by NEOS Technologies, the scanners and optics are integrated into a single unit. This unit, built with off-the-shelf components, provides multi-beam AO scanning, which allows the projection of 40,000 voxels at a refresh rate of 20 Hz and an x–y spot resolution of 256 $\times$ 256. An improved interface control card, VDRG2, was designed and fabricated at SSC San Diego to support the new scanner.

The development of a second-generation AO scanner, with its improved voxel-generating capability, produced a need for a larger volume helix to explore and evaluate its full potential. A 36-inch engineering development model was designed to meet this challenge. Fabrication costs and safety issues made its development using the same methods as with the smaller systems impractical. Hence, a decision was made to fabricate this large helix from polystyrene plastic. This polymer was selected primarily for its light weight and relative ease of production. The choice of polystyrene was also influenced by its availability in transparent and translucent forms. This option would allow it to serve, in the interim, the development of the next-generation helix in which laser images are projected onto it from its backside.

Figure 2-3 shows the second-generation system. Because of its walk-around design, the laser beam producing the image must be projected onto the helix from overhead. This is accomplished in the laboratory by using mirrors suspended from the ceiling to reflect the signal being emitted by the AO scanner. The beam deflecting range of the AO scanner is limited to approximately 10 degrees, meaning that the beam must travel approximately 16 feet from the scanner to the helix if it is to be able to create images anywhere in the display volume. The mirrors are located such that they fold the laser signal, adding the necessary length to its travel distance.

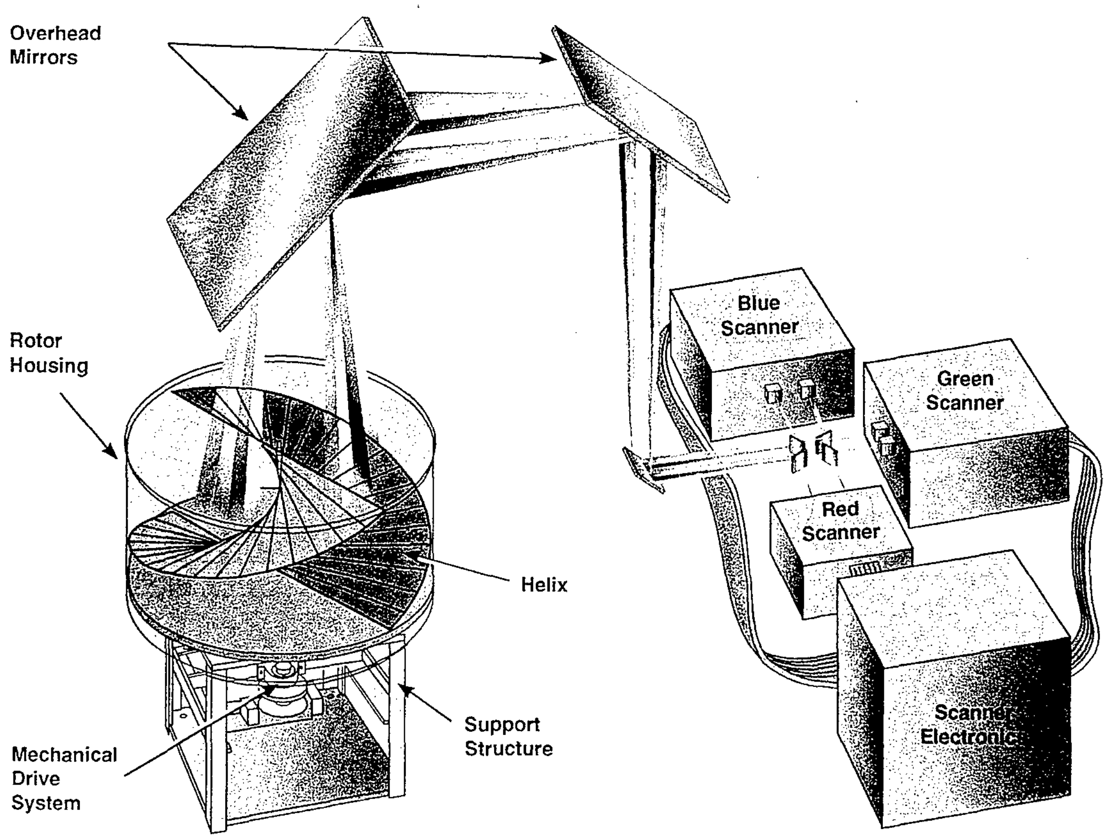

Figure 2-3. Second-Generation 3-D Volumetric Display System (laboratory model).

Figure 2-4 shows the 36-inch helical display assembly expanded into its major components. The major components are: the helix, the rotor housing, the bearing and support structure, the mechanical drive system, and the angular position sensor and the safety shield. Each of these is described here in detail.

1.3.1. Helix

When rotated, the interim helix displaces a cylindrical volume 36 inches in diameter and 18 inches high, providing a potential imaging volume of 10 cubic feet. The upper surface of this helix, as in the preceding models, acts as the display field and follows a true helical contour having a pitch equal to 36 inches. The upper surface is treated with an opaque white finish, so that it must be illuminated and viewed from the same side. The blade has a uniform thickness of 2 mm, except for a half-inch diameter cylinder concentric with its vertical axis to accommodate a center pin. The helix is assembled by vertically stacking 18 1-inch-high injection-molded plastic segments, and the pin is used to align their

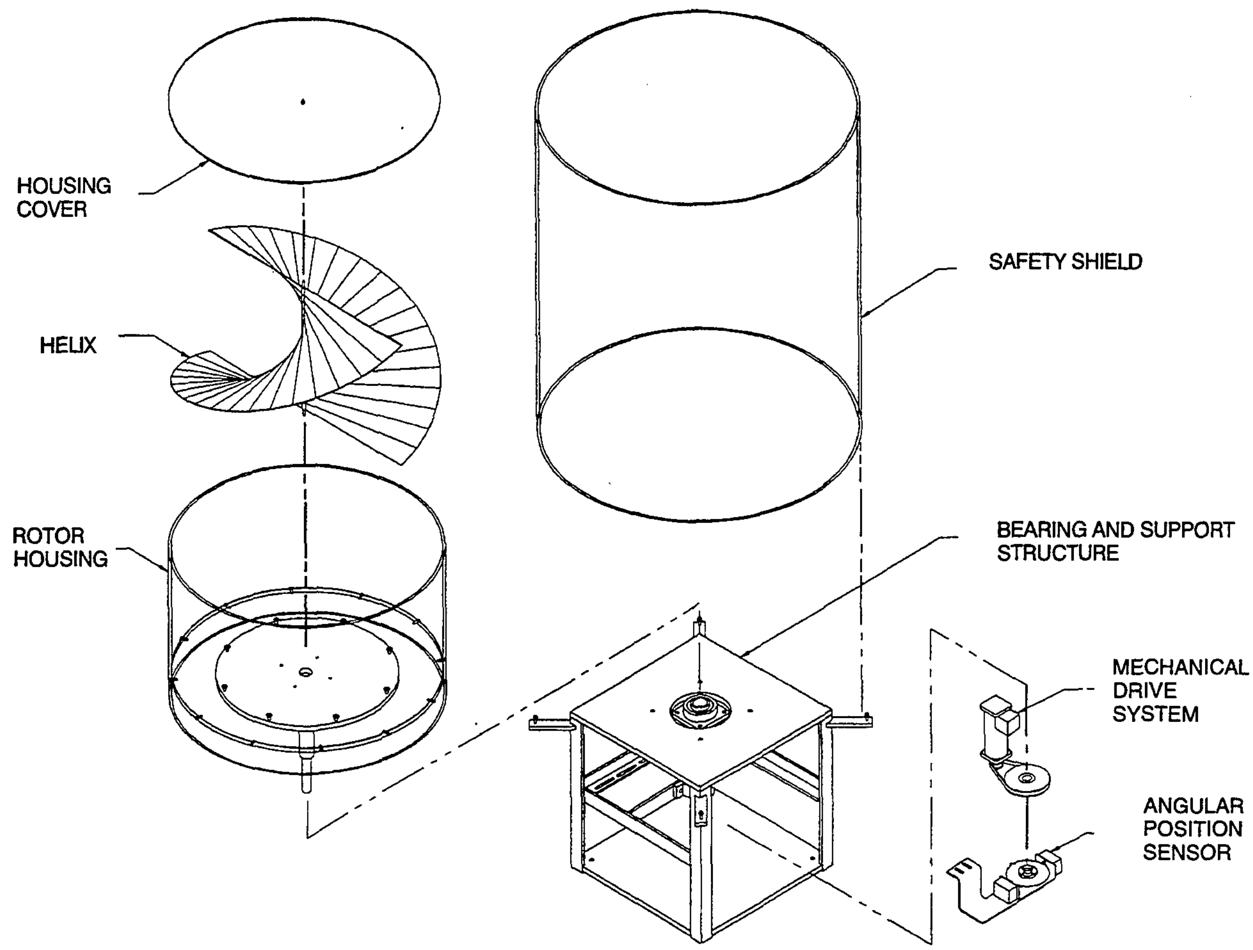

Figure 2-4. Interim model helical display: major components (expanded view).

centers until they are bonded together into a continuous helical blade. The steel pin also provides a simple and accurate datum for centering the helix in its housing. The pin does not interfere unduly with image generation since use of that area of the helix is avoided. The steepness of the helix near its center may cause elongation and distortion of the laser spot, making this region difficult to use. For this reason, the primary areas selected for the creation of images are typically located midway between the center and rim of the helix. The helix and pin weigh 5.0 pounds.

1.3.2. Rotor Housing

The interim helix is fully enclosed in a transparent cylindrical housing that rotates with it. The helix is mounted about its entire perimeter against a locating ridge on the inner wall of the housing and secured by acrylic clamping strips. While the housing provides a measure of safety to the helix by preventing inadvertent contact with nonrotating objects, its primary function is to rotate the volume of entrained air, alleviating the plastic blade of the drag load and structural stresses that it would otherwise experience. The main body of the housing is a 36-inch diameter, 24-inch tall acrylic cylinder fitted with a removable top plate. The housing is mounted on a circular aluminum turntable bolted to the top end of a vertical steel shaft. These components spin together in a pair of shaft bearings as a single unit, referred to as the rotor assembly. Auxiliary components of the rotor assembly include a

drive pulley, an encoder disk, and counterweights used to dynamically balance the assembly. The total weight of the interim system's rotor assembly is 125 pounds.

The structural stiffness of the rotor is critical to its smooth performance. If rotational speeds approach the first natural frequency of the rotor assembly, a resonant condition may occur. The rotational speed at which this condition occurs is referred to as the first critical speed of the rotor. The rotor should not be operated at or near its first critical speed. By dynamically balancing the rotor, however, deflections and forces may be sufficiently reduced so that it is possible to approach or even run through the first critical speed without noticeable disturbance.

1.3.3. Bearing and Support Structure

In the second-generation system, the stepped rotor shaft is supported by a pair of compact antifriction bearings. The weight of the rotor is carried by a flange-cartridge, self-aligning angular contact bearing unit near the top of the shaft. Radial loads are shared by the flanged unit and a smaller pillow-block-mounted, self-aligning bearing near the bottom of the shaft. This bearing arrangement minimizes machining requirements and simplifies mounting and leveling of the rotor. Close tolerance fits at the shaft/bearing interface are essential to eliminating noise. The shaft, bearings, and bearing foundations are of sufficient size and rigidity to isolate the main body of the rotor from the drive components and the vibration associated with them, resulting in its relatively quiet operation.

The bearing foundations and supporting structure are constructed from aluminum angle and plate, joined in a single weldment to maximize rigidity. The first natural frequency of the weldment is designed to be considerably greater than the excitation frequency of the spinning rotor to avoid resonant vibration. The frame provides mounting plate foundations for the motor and angular position indicator. Its base has provisions for leveling and securing the framework to the floor or supporting foundation. This feature adds structural rigidity to the frame and assures that optical alignment is maintained, preventing image distortion.

1.3.4. Mechanical Drive System

Motive power is conveyed to the rotor shaft through a cogged belt and pulley arrangement by a 1/2-horsepower dc motor. The motor, operating at a nominal speed of 2400 rpm, maintains the constant speed of the rotor through a 4:1 pulley arrangement. The motor is supported by a remotely located computer-controlled 60-amp dc power supply.

1.3.5. Angular Position Sensor

The angular position of the helix is monitored by an optical encoder designed and fabricated at SSC San Diego. The position of the helix is sensed twice per revolution through a pair of optical switches located on opposite sides of the rotor shaft, 180 degrees apart. A tab on a shaft-mounted trigger disk provides an interrupt signal as it rotates through each switch. This signal provides reference location and rotational speed data from which angular position is inferred by the processor.

1.3.6. Safety Shield

A 42-inch diameter, 48-inch high-impact-resistant safety window, comprised of a polycarbonate-laminated acrylic cylinder, surrounds the rotating display unit. This window allows close-up walk-around viewing of the helical display while preventing inadvertent contact between the observer and

the spinning rotor. The window is designed to contain high-speed projectiles if a component breaks away from the rotor.

1.3.7. Dynamic Balancing

It is essential for its smooth operation that the rotor assembly be balanced. The purpose of balancing is to eliminate the centrifugal force that arises from the eccentric rotation of the center of gravity (cg) of the rotating components about the axis of rotation. These oscillating forces and the resulting stresses set up by them are transmitted through the rotating components to the bearings and support structure, with results that may range from noise and vibration to catastrophic failure. As rotor speed is increased, a sequence of events is initiated by any imbalance in the system. The eccentricity of the cg location will cause the rotor assembly to experience a net centrifugal force that, in turn, results in additional radial deflection of the cg away from the axis of rotation and an increase in the amount of imbalance. This cyclical escalation in the degree of imbalance progresses until the correcting spring forces in the support structures reach an equilibrium with the centrifugal forces. If the induced stresses in the structures exceed their design limits before an equilibrium is reached, the structure may fail. A nonlinear force-deflection response of the structure, in which stiffness is reduced as the deflection is increased, may produce an instability which will lead to catastrophic failure.

In theory, any state of rotor unbalance can be reduced to two basic components, a force and a moment; two separate balancing planes are all that is required to counter the effects of both. A rotor is considered rigid if it can be balanced in any two arbitrarily selected axial planes and maintain this state of balance throughout its operating-speed range. For all practical purposes, the helical display is treated as a rigid rotor. The two-plane method of balancing is referred to as dynamic balancing because, in addition to countering the static force produced by a cg eccentricity, it also compensates for the moment that is generated only during rotation.

The rotor assembly is balanced on a balancing machine. The rotor is removed from its bearings and mounted horizontally in the device. It is rotated at its design speed and vibrational data is gathered through the machine's bearing mounts. The data are processed and balancing instructions are indicated on the machine's console. Balancing is achieved by attaching lead or acrylic weights to the rotor assembly in two planes: the underside of the rotor baseplate and the upperside of the top plate. The counterweights are carefully located against the inner wall of the rotor's cylindrical body so that they will continue to be retained and not become projectiles if they become unattached. To avoid visual disruption caused by counterweights in the field of view, an offsetting counterweight is attached in a strategic location inside the cylinder, but below the helix and out of view. This reduces the requirement for counterweights in the top plane so that only small acrylic blocks are needed there for fine adjustment.

2. THE TRANSPORTABLE SYSTEM

With the second-generation system successfully demonstrated in the laboratory, the 3-D Volumetric Display System team started work on the next-generation concept, a transportable system. The transportable model was developed to allow the 3-D display system technology to be demonstrated outside of the laboratory and to facilitate exploration and field testing of potential applications. A number of uses for this technology having military, medical, and commercial applications have been suggested.

A number of design changes were made to make the system mobile. The change having the greatest impact on the design of the helix was the removal of the large, overhead mirrors and their replacement with much smaller mirrors located below the helical display. Rear-projection techniques were used to illuminate the helix. Laser signals emitted by the scanner were folded to the proper projection length in a sublevel system of mirrors and directed upward onto the underside of the helix. The images, projected from below, are visible from above. This approach allows the complete optical system to be packaged as an unobtrusive unit that can be moved with very little reassembly or realignment required. To accommodate rear projection, the helix must be translucent or semitransparent so that it totally diffuses the incident laser beam and creates a spot that is clearly visible, but not hazardous to the viewer. Ideally, half of the incident light is transmitted through the helix and the other half reflected back, making the voxels visible from the topside and the bottomside with equal intensity.

Materials having suitable optical, mechanical, and producibility characteristics for fabricating the translucent helix were identified after testing and evaluating many candidates. An initial sampling of commercially available translucent materials proved most of these to be unsuitable. The material demonstrating the best balance of desirable qualities and judged to have the most potential for development in this application was determined to be transparent polethylene (PETG) plastic sheet, vacuum-formed to the proper shape and surface-treated with a combination of sand-blasting and titanium dioxide paint to obtain the desired optical qualities.

The preliminary goals established for the transportable design included a 36-inch helix with three-color imaging (red, blue, green), 40,000 voxels per color, and color convergence. The display volume for this design requires approximately 1 W of optical output power for each color, establishing a requirement for water-cooled lasers. Each of the lasers selected to fill this need requires approximately 22 kW of power and a 220-VAC three-phase power source. The external cooling unit needed to support the lasers will also require 220 VAC. The weight of the this system was estimated to be 1500 pounds and its estimated power consumption was placed at 45 kW. The weight estimate and power consumption and source requirements were deemed unacceptable for a transportable system. A more acceptable design was sought.

Solid-state lasers typically require a common 115-VAC power source and only air for external cooling. This makes them preferable to water-cooled lasers in the packaging of a transportable system. The solid-state units have an optical power output of only 100 to 200 mW, however, and an efficiency of only 30 percent. To make this design workable, the display volume and, thus, the helix size, would have to be reduced in proportion to the optical power reduction. This would restore voxel intensity to an acceptable level. A decision was made to reduce the size of the helix to 12 inches in diameter by 6 inches high for the transportable system.

The reduced size of the helix also facilitates transportability requirements that demand the system be capable of being dismantled into subassembly units that can be easily managed and shipped. The physical characteristics of each of these subassemblies allow them to be lifted and moved without requiring special equipment, to pass through a 36-inch doorway and to withstand the rough handling expected during shipment by conventional freight carrier. The rotor and safety shield must also be removable from the display base for packaging in a separate container during shipment. The transportable system is comprised of three main assemblies: 1) the helix support assembly; 2) the laser scanner assembly; and 3) the electronics assembly. Figure 2-5 illustrates this configuration.

Figure 2-6 shows a cut-away view of the helix support and laser scanner assemblies. The helix support assembly houses the framework and bearings that support the helix and rotor assembly, the drive

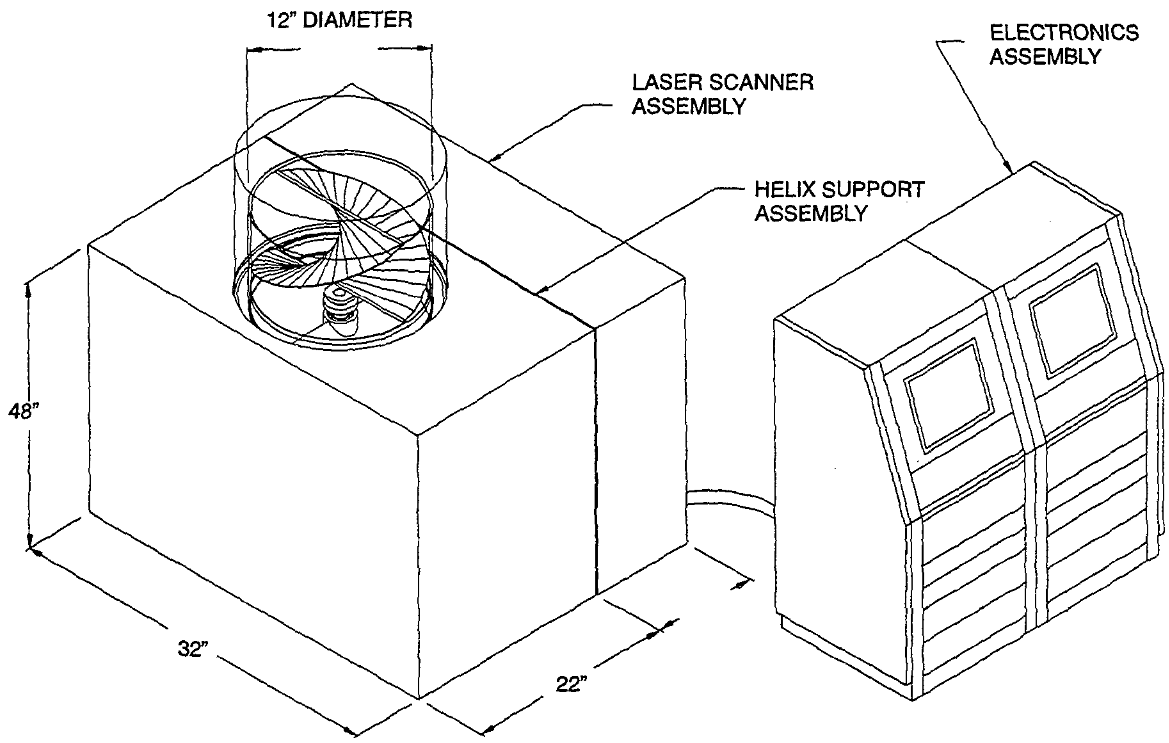

Figure 2-5. Transportable 3-D Volumetric Display System.

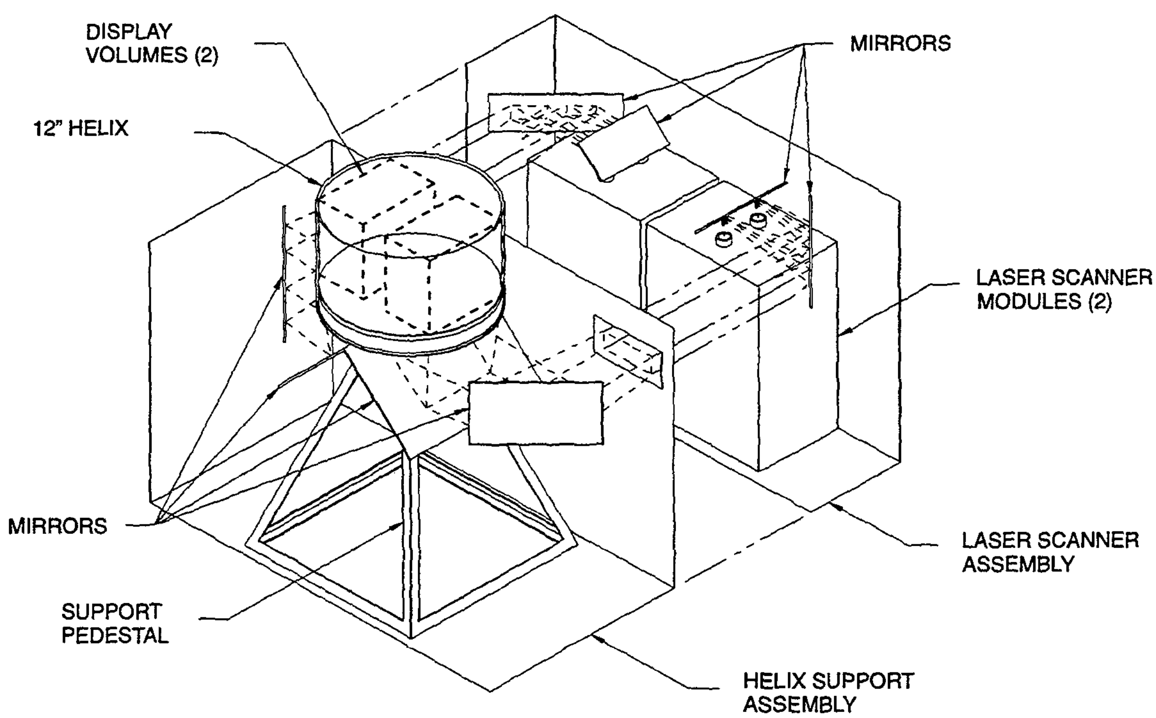

Figure 2-6. Transportable display: component arrangement.

motor and drive components, the position sensors and the final stage mirrors. The rotor assembly may be removed from the support assembly for shipping. The helix support assembly has an aluminum frame structure and an independent aluminum structural shell to seal out dust, isolate the frame from contact by observers, dampen motor noise, support a safety window, and enhance overall appearance. The laser scanner assembly houses the lasers, scanners, scanner drivers, power supplies, projection lenses, and beam-folding mirrors. This assembly also contains a rigid aluminum framework, on which a number of its components are isolation mounted, and an independent aluminum shell. Both of these assemblies have alignment keys and mating windows to allow them to be joined together for operation, but separated during transport. The electronic cabinet assembly houses the computer, power supplies, and RF drivers for the 40,000 voxel scanners. The electronic cabinet is constructed using a commercially available electronic enclosure and is air-cooled. It is connected to the two other assemblies via electronics cabling. The system requires a 2-kW, 115-VAC power source. Each of the three assemblies weighs approximately 400 pounds.

The design of the rotor housing is similar to that in the second-generation model. Its base, however, is transparent to allow laser signals to pass through from below. A long steel shaft supports the rotor in its bearings.

The transportable helix is supported by a pair of self-aligning cartridge bearings located 12 inches below the cylindrical housing.

The rotor shaft is designed to allow easy removal from its bearings and to facilitate packing of the rotor assembly in a shipping container. Motive power is provided to the rotor shaft by a 1/2-horsepower DC motor.

To allow laser signal access to the underside of the rotor housing, the bearing support framework is arranged in a pyramidal configuration. This design allows the projection-folding mirrors to be positioned directly below the rotor and adjacent to the shaft, making most of the helix accessible for imaging. The framework rigidly supports the bearing units and extends to the base of the system to provide firm coupling with the supporting foundation.

The ability to write to the entire volume of the shaft-driven helix is restricted by the shadow of the shaft and by the supporting framework. This is handled by writing to two display volumes on opposing sides of the helical axis. Each of the two display volumes is $5 \times 5 \times 6$ inches in the arrangement shown in figure 2-6.

The transportable system is very flexible in its design and has been used as a test bed for new designs and configurations. In a simplified configuration having only a single solid-state laser, the laser and scanners are relocated directly below the helix. The size of the overall system is reduced by the elimination of the laser scanner assembly housing The weight of this simplified system is reduced to approximately 200 pounds. In another test configurations, the double-helix blade is replaced by a single helix driven at 1200 rpm.

3. DISCUSSION

Advances in computers, lasers, and AO scanners have made the unique technology used in the 3-D Volumetric Display System practical only in recent years. The helical displays discussed in this paper provide a mechanical method for exhibiting these scanner-generated, three-dimensional images but are not by any means the only mechanism for achieving this effect. Rare-earth solid-state matrices, rotating flat plates, and oscillating pistons are three methods concurrently being investigated as alternate display mediums. The technology used in helical displays, however, has been successfully demonstrated in the laboratory and the engineering developmental models discussed here, have, thus far, proven themselves capable of revealing the potential of the most recent laser/scanner systems.

The smaller helix, previously discussed, serves as a laboratory test platform for investigating new applications where small imaging volumes with a reduced number of voxels is acceptable. It allows the refinement of translucent helix materials and rear-projection methods, the development of alternate bearing designs, and the exploration of size-reduction techniques. NEOS Technologies has developed a combined scanner/laser and accompanying RF drive electronics in a teaming effort with SSC San Diego. This new design provides enhanced performance while permitting further size reduction of the laser scanner assembly. Both of these efforts have benefited the design of the transportable system.

In meeting the needs of the system, each new development model has addressed an ever-increasing number of design requirements that include larger sizes, higher speeds, noise suppression, drag reduction, dynamic balancing, safety assurance, portability, and optical compatibility (i.e., light-diffusing). New developments in system components, software, and applications are likely to create new requirements for helical display components. Some of these being anticipated and currently being studied are for large-diameter bore bearings, greater precision helix surfaces, the ability to resolve RGB color, and high-strength, impact-resistant helix materials. The incentive to meet design challenges has, thus far, been the need to demonstrate the feasibility and potential of the system. These new capabilities will expand its envelope of applications. Efforts to develop these new capabilities have been, for the most part, limited to preliminary investigations and feasibility studies while sponsorship is solicited. It appears that the evolution of the helical display will depend on the manifestation of a need or application.

SECTION 3. 3-D ELECTRONICS

Weldon Dahlke, Electronic Control Cards and Circuit Design Lead Engineer.

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SECTION 3. 3-D ELECTRONICS

1. INTRODUCTION

The Space and Naval Warfare (SPAWAR) Systems Center, San Diego (SSC San Diego) in San Diego, California, is developing a 3-D Volumetric Display System for data, information, and scenes in a three-dimensional volume. Code D44, the Simulation and Human Systems Technology Division, has designed a system that incorporates a 13-inch-diameter double helix (first generation), and a 36-inch-diameter by 18-inch-high double helix (second generation), spinning at approximately 10 revolutions per second. Under computer control, a laser beam is directed to illuminate discrete volume points (voxels) on the helix as required by the scene being created.

Refresh operation is made independent of the computer speed by an electronic interface card called the "Volumetric Electronic Personal Computer (PC) Control Card." This multilayered interface card can address up to 12,288 points (voxels) for the first-generation card (volumetric #1) and up to 65,536 points (voxels) for the second-generation card (volumetric #2).

Flexibility is built into this card through numerous test points and optional jumpers. Section 2 provides nominal settings for operation of the interface card with the NEOS 40K voxel scanner along with the source and destination of important signals.

A complete parts listing showing the device board and schematic location is included in section 3 to facilitate troubleshooting, maintenance, and repair.

Section 3-2 is a complete part-by-part inventory useful for new board construction. The listing provides a list for purchasing or kitting.

The appendix contains a comparison of volumetric #1 and #2 cards plus complete schematics and layout drawings of the Volumetric #2 PC Interface Card. The first-generation volumetric #1 card can store 12,288—24-bit voxel words, while the second-generation volumetric #2 card can store 65,536—32-bit voxel words.

2. GENERAL PURPOSE

The volumetric #2 card is designed to allow a PC to accurately control the position of a single laser beam on a moving surface to form a 3-D image. The volumetric card synchronizes the laser beam to a double blade helix (angular rotating surface) or to a piston (reciprocating surface) to generate the depth. The reflection of the laser beam from the diffused moving surface of the helix or piston provides a true 3-D display with viewing angles up to 180 degrees without using polarizing glasses.

3. BACKGROUND

A true 3-D display has been constructed at SSC San Diego. The display surface is a rotating 36-inch-diameter double helix with an 18-inch depth that is simultaneously written on by one or more laser beams. Each laser beam is deflected in X and Y using the property of Bragg defraction in acousto-optic crystals. An acousto-optic modulator inserted in the laser's optical beam path provides a means for the computer to control the intensity of the image on a voxel-by-voxel basis.

The volumetric #2 control card is the interface between the computer and the acousto-optical system that directs the laser beam. Image coordinates are stored in the card's memory. The depth is determined by synchronizing the image data readout from port "B" of the dual-port memory to the position of the helix surface. Timing signals from the double-helix shaft at 0 and 180 degrees are used to reinitialize the memory readout to the beginning of the image. Figure 3-1 shows a simplified diagram of the 3-D Volumetric Display System.

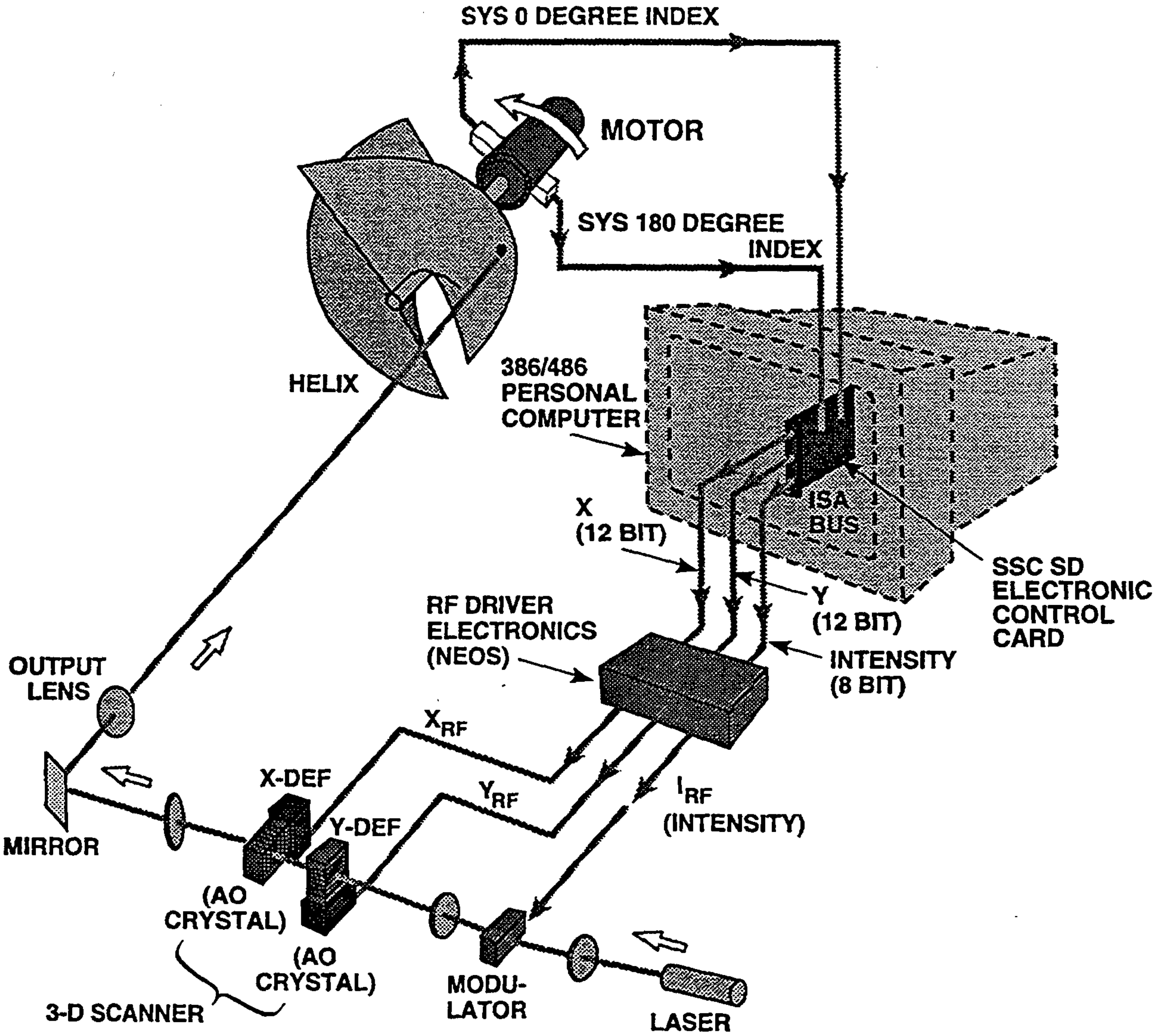


Figure 3-1. Simplified 3-D Volumetric Display System.

4. FUNCTIONAL DESCRIPTION

Figure 3-2 is a simplified functional diagram of the volumetric #2 control board. Reference to this figure will be helpful for the following descriptions.

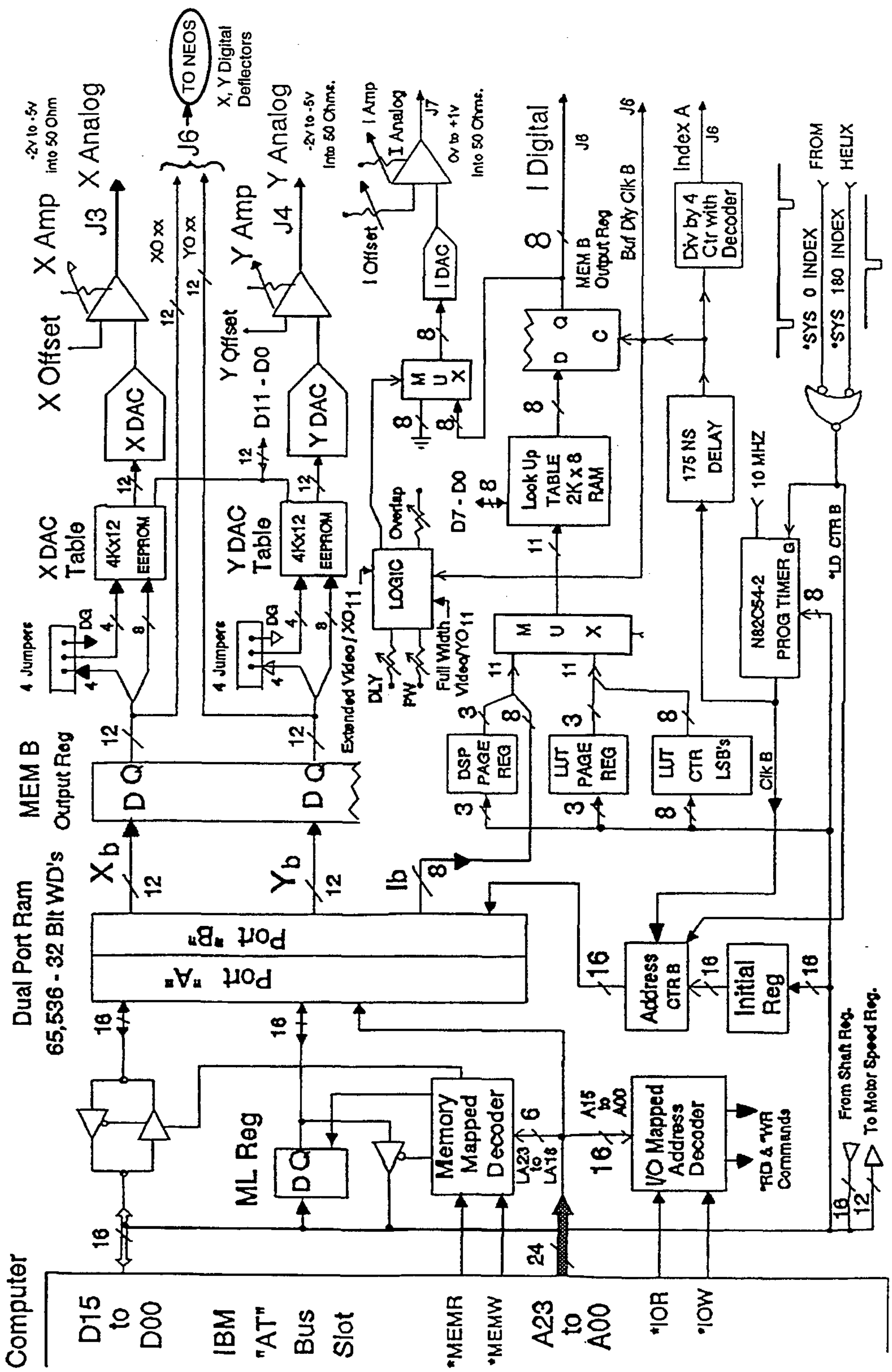


Figure 3-2. Simplified SSC San Diego volumetric #2 card.

4.1. DUAL-PORT MEMORY

Dual-port random-access memory (RAM) is used to hold the data on the individual points of the image to be displayed. These 2-D points are transformed to voxels (3-D points) when the laser beam strikes the moving surface of the helix. The points position in the image list relative to the position of the helix surface at readout time determine the depth.

The volumetric #2 board has a dual-port RAM memory that holds up to 65,536—32-bit words. Each word defines a point that has 12 bits for X and 12 bits for Y (4096 by 4096 addressability), 8 bits of intensity (255 levels of video plus blanking [all zeros]). The X11 position is either X11 most significant bit (MSB) or Extended Video, while the Y11 position is either Y11 (MSB) or Full Width Video, depending on the setting of manually adjustable jumpers. (See figure 3-3.)

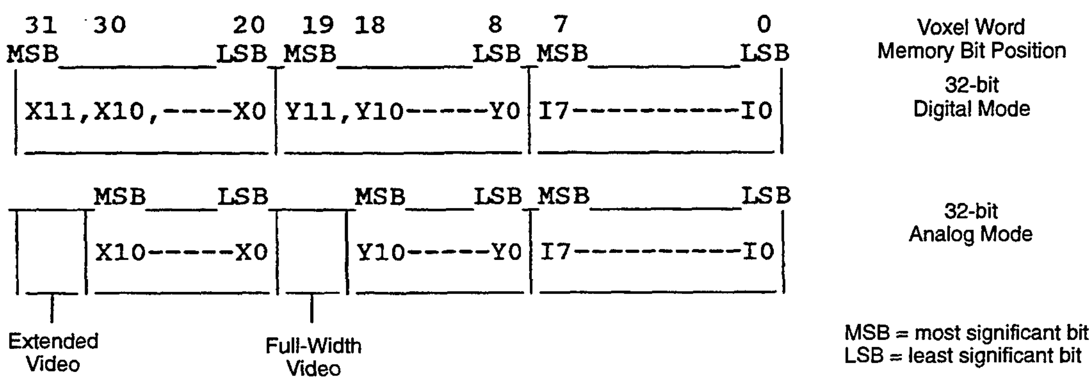


Figure 3-3. Voxel word memory formats.

The dual-port RAM provides two independent ports (A and B) with separate control, address, and data buses that permit *independent asynchronous access* for writes and reads to any location in memory. This property allows writing data into port A at the "computer's" rate while simultaneously reading out an image at port B at the desired helix or piston's data refresh rate.

Port "A" of the dual-port memory (PC side) is direct memory mapped. A 256-kb address block in the 1-MB to 16-MB address range of the host computer is used for this purpose. This allows faster data transfers than the input/output (I/O) memory commands used in the volumetric #1 card.

Equal time slices are allotted for each point or voxel in the 3-D display image. The points in the image are sequentially read from port "B" of the memory starting with the address held in counter "B." Counter "B" is reloaded with the beginning value held in the initial register whenever the helix shaft reaches 0 or 180 degrees. The address counter "B" always increments in the helix mode. When a piston is used, the address counter "B" initially starts incrementing at 0 degrees then reverses direction at 180 degrees to begin counting down.

The port "B" beginning address is loaded into counter "B" from the initial register whenever a *System_0_Index or a *System_180_Index (* indicates active low true logic) is received from the double-helix shaft sensors. This arrangement allows different memory pages to be displayed by just changing the value in the initial register. Typically, the 3-D memory is configured as sixteen 4K or eight 8K pages.

Provisions are also incorporated in the design to work with a piston through selectable jumpers. When the piston mode is chosen, the *System_0_Index signal would reinitialize the memory readout to the beginning of the image and start to count up as before. However, the *System_ 180_Index signal will now cause the address counter "B" to reverse direction and begin to count down.

The data "B" readout rate from memory is under computer software control via the 82C54-2 programmable timer. Valid readout periods are integral multiples of the timer 10-MHz clock input or N x 100 nanoseconds with n>1.

If n = 13, the readout rate is 1.30 microseconds per each voxel allowing up to 38,461 different voxels to be read and displayed in 1/20 of a second.

Counter 0 of the 82C54-2 timer is normally programmed to mode 2 (divide by N mode) with N = 13 to periodically produce a 100-nanosecond active low pulse every 1.30 microseconds for memory readout.

The image refresh rate has been nominally selected at 20 Hz. This is a compromise between displaying more image voxels per frame and image flicker. A lower refresh rate allows more voxels to be displayed per frame but causes excessive flicker. Increasing the brightness of the image also causes flicker unless the refresh rate is increased.

Twelve bits of X and 12 bits of Y are read from port "B" of the dual-port RAM and are sent to the Newport Electro-Optics Systems (NEOS) computer interface controller board for each voxel (via J6). This board converts the signals to 16-bit X and Y coordinates, which drive separate digital X and Y RF synthesizers feeding each of the acousto-optic laser deflection crystals.

Analog voltages of X (J3) and Y (J4) are also generated on the volumetric #2 board. Analog X and Y voltage corrections are easily made since the X and Y digital words are first processed by their respective EEPROMS before being converted to analog form. Separate offsets, amplitude controls, and individual programming of the EEPROMS allow waveforms with a 5-volt maximum swing (i.e., 0 to +5 V, 0 to –5 V, –2.5 to +2.5 V, etc.) into 50 ohms to be generated.

4.2. INTENSITY OUTPUT

An acousto-optic (AO) modulator (see figure 3-1) inserted into the laser's optical beam path provides a means for the computer to control the intensity of the image on a voxel-by-voxel basis.

The intensity output provides the controlling signal for the acousto-optic modulator to vary the intensity of the incoming laser light beam into the X and Y acousto-optic deflection crystals.

Digital Intensity (8 bits via J6) as well as an Analog Intensity voltage (+1 V max into 50 ohms at J7) are generated for each voxel.

The Analog Intensity output is a gated analog signal (one of 256 possible levels from 0 to +1 V) with various pulse widths. The analog amplitude and various pulse widths of each voxel are individually programmed from 10 bits in the voxel's memory word. Eight bits are for intensity amplitude control while the other two bits combine to generate various intensity output pulse width modes.

The MSB of digital Y (Y11) is used for individual voxel Full Width Video control instead of its normal Y (MSB) function. The MSB of digital X (X11) is used for Extended Video control instead of

its normal X (MSB) function. This method allows full Analog Intensity control along with 2048 addressability of digital X and Y.

The Full Width Video control bit and Extended Video control bit combine to select one of three pulse width categories that are

a. Fixed Pulse Width (PW) mode. See figure 3-4, Waveform E under Md1 column and Case 1.

b. Extended Video mode. See figure 3-4, Waveform E under Md2 and Md3 and Case 2.

c. Full Width Video mode. See figure 3-4, Waveform E under Md4 and Case 3.

(Refer to the description of intensity video output timing diagrams under Case 1, Case 2, and Case 3 for additional information following the diagrams).

Various combinations of intensity, extended video, full video, PW, blanking, and voxel readout rates give the programmer of the volumetric card many options in which to vary the intensity of each voxel in the final image.

```
                                   X1,Y1       X2,Y2         X3,Y3         X3,Y3
Waveform A.                      |----------|-----------|-----------|-----------|
Sequential Data Words (Mdx)         Md1         Md2          Md3          Md4

Waveform B.                                   ( V2 )
Memory Word                V2-     ( V1 )   |-----------|   ( V1 )       ( V1 )
Intensity Field (8 bits)   V1    |----------|           |-----------|-----------|
Converted to Analog         0    |                                              |
Voltage

Waveform C.               ON-    |          |           |           |-----------|
Full Width                 0-    |----------|-----------|-----------|           |
Video Control

Waveform D.               ON-    |          |-----------|-----------|-----------
Extended                   0-    |----------|                       |-----------|
Video Control
                                                 Ext Vid
                           V2-        PW        |------|       Ext Vid   Full Width
Waveform E.                V1-        |---|                  |------|-----------|
Intensity                  0-    |---|    |--|----|     |----|                  |
Output (J7)                       Dly          Dly          Dly          No Dly
                                 |- Fixed --|-Extended -|-Extended -|-- Full ---|
                                 Pulse Width   Video        Video     Width Video
                                    Mode       Mode         Mode
```

Figure 3-4. Intensity video output timing diagrams.

4.3. DESCRIPTION OF INTENSITY VIDEO OUTPUT TIMING DIAGRAMS

Waveform A in figure 3-4 shows four sequential memory digital words (Md1, Md2, Md3, and Md4) with their X and Y fields defining the coordinates of their respective points.

Note: Md3 and Md4 are two sequential memory locations that are effectively combined to create a broader point with increased brightness. Both points have the same X and Y point coordinates

(X3,Y3) but differ slightly in depth due to the rotation of the helix surface since Md4 follows Md3 slightly in time.

The time (Mdx) available for each digital word read from memory is calculated as follows:

Memory digital word = Md = (1/refresh)/ # of displayed voxels.
Md = (1/20)/38,461 voxels = 1.3 microseconds per voxel at a 20-Hz refresh rate.

In figure 3-4, Waveform B shows the 8-bit intensity fields of each memory digital word (Md1, Md2, Md3, and Md4) converted to their respective analog intensity voltages (one of 256 levels from 0 to +1 V) labeled V1 and V2.

In figure 3-4, Waveform E shows four cases of the Intensity Analog output resulting from various combinations of the Full Width (Waveform C) and Extended Video (Waveform D) control bits when applied to the memory words Md1, Md2, Md3, and Md4.

Case 1. Fixed Pulse Width (PW) Mode (figure 3-4, Waveform E under Md1 column)

The Full Width and Extended Video control bits are both low, as shown under memory word Md1 for this mode. This causes the intensity output to be blanked (0 V) for a delay (Dly) period to eliminate video smearing when changing from the X,Y coordinates of one point to another, then shifts the video to the analog level V1 for a fixed PW time period. The video then shifts back to ground or the blanking state for the remainder of the memory word (Md1) period.

Video intensity fixed PW (figure 3-4, Waveform E) is adjustable and currently is manually set to a nominal value of 500 nanoseconds. This video PW remains constant at the selected value even if the number of voxels read out is reduced, thereby increasing the time between memory words.

The *intensity delay* (figure 3-4, Waveform E) is manually adjustable and is used to blank out the video for a fixed time period each time a voxel is read out. The intensity delay is nominally adjusted to equal the optical access time (T) or fill time of the deflection crystal to eliminate video smearing when changing between voxels with different X and Y Coordinates.

Note: The optical access time or fill time is defined as the time required for a new RF frequency (new X or Y position) to enter the AO scanner deflector crystal and propagate across the laser beam.

T(optical) = laser beam diameter into deflector crystal/acoustic wave sound velocity.

T = 6.35 mm / 0.617 mm per microsecond = 10.29 microseconds for the NEOS 256 by 256 resolution on-axis TeO_2 slow shear crystal scanner.

Case 2. Extended Video Mode (figure 3-4, Waveform E)

The Full Width control bit is low and the Extended Video control bit is high (shown under memory word Md2 for this mode). This causes the intensity pulse to go to the appropriate analog level (V2) after the delay period and to stay at that level until the next voxel is read out. The Extended Video bit, in effect, extends the width or on time of the fixed PW pulse.

Case 3. Full Width Video Mode (figure 3-4, Waveform E)

The Full Width Video control signal overrides the Extended Video control signal causing the delay time to be eliminated, thus allowing the intensity output to go to the appropriate analog level (V1) for

the whole duration of the memory time (Md4 in this case) regardless of the Extended Video control signal's level.

Case 4. Increasing the Intensity of a Point, Method 1

An Extended Video word followed by a Full Width word with the same X and Y point (X3,Y3) as shown in Md3 and Md4 effectively allows generation of a much brighter point without video smearing or increasing the power of the laser. If the Dly is 90 percent of the voxel period, the resulting brightness increases by a factor of 5.5 over two adjacent Extended Video voxels. This technique does increase the brightness of the combined point, but it uses two memory words per point, thus decreasing the number of separate points in the image.

Case 5. Increasing the Intensity of a Point, Method 2

The brightness of each voxel can be increased if the Extended Video bit is enabled and the number of voxels read out is reduced, thereby increasing the time between memory words and thus extending the video PW of the remaining voxels. However, this method does have a trade-off in that fewer points of the image can be displayed during the allotted refresh time.

Case 6. Blanking of the Laser Beam

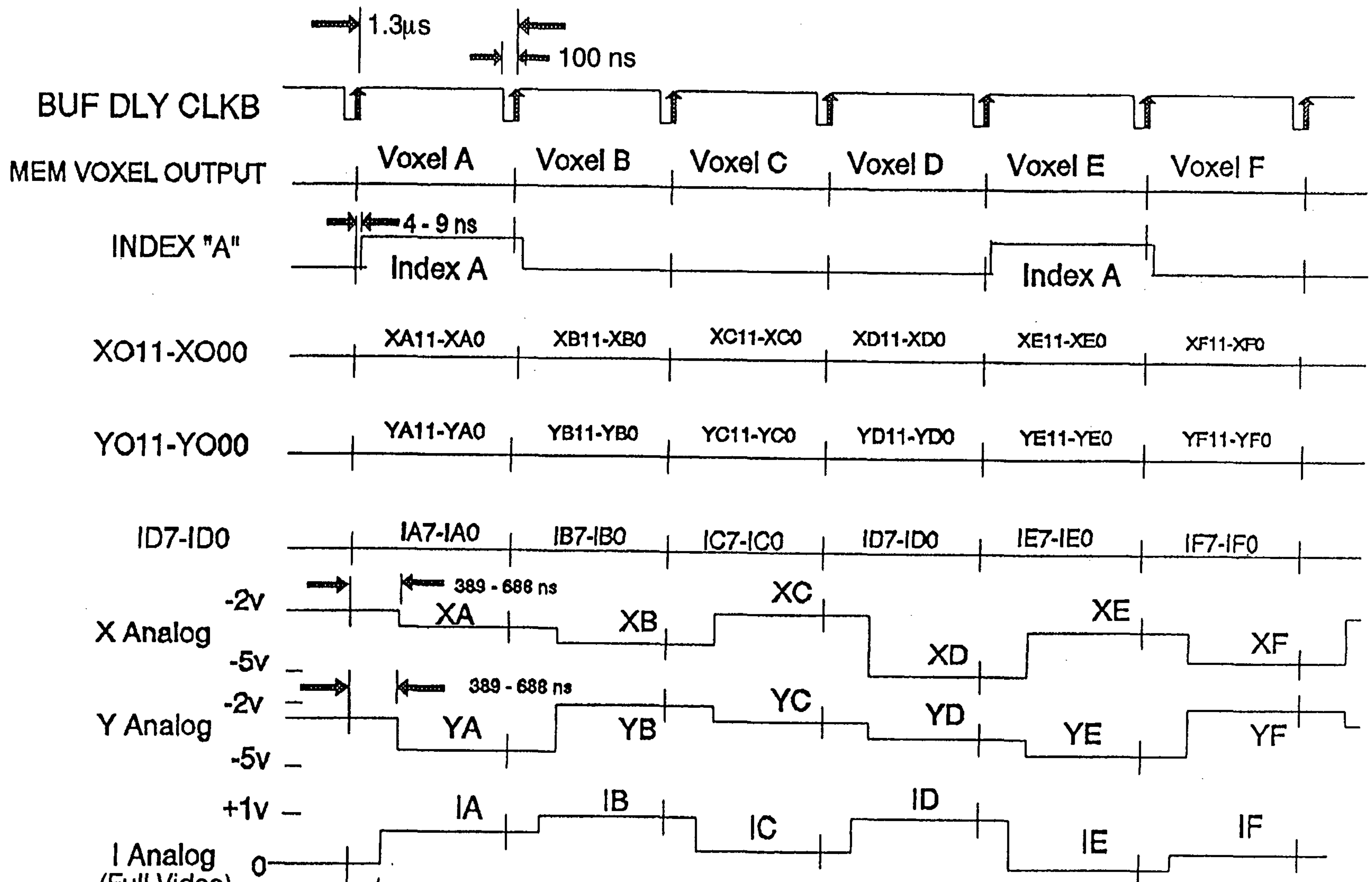
Blanking occurs whenever the intensity output voltage is 0 V. Blanking occurs when the 8 intensity bits in the memory word are zeros or whenever the logic shifts the intensity output to ground (i.e., during intensity delay and after the duration of the fixed width pulse has occurred).

4.4. VOLUMETRIC #2 TIMING

Figure 3-5 is a reference diagram that shows the volumetric #2 timing for six sequential voxels.

4.5. MOTOR SPEED CONTROL

The motor speed control regulates the speed of the 3-D display's shaft. The computer sends a 16-bit word to the motor register, the lower 12-bits are converted by a 12-bit digital-to-analog converter (DAC) to furnish a nominal 0 V to +10 V maximum control signal to the helix motor power supply. The analog voltage (E_motor) can be adjusted via R28 to supply +5 V maximum when the code 0FFF hex is sent from the computer.



NOTE: X000, Y000, ID0 are the Digital LSB's of X, Y and I,
Use X011 – X000 and Y011 – Y000 for the 40K Voxel 256 by 256 Scanner

Figure 3-5. Volumetric #2 timing.

4.6. MOTOR SHAFT'S ACTUAL SPEED DETERMINATION

The shaft speed circuitry accurately determines the helix actual shaft speed without an expensive shaft encoder and takes a minimum of computer time. The computer can read the shaft register at any time, and by multiplying this count by 6.4 microseconds (period of the selected 156.25-kHz shaft counter clock), one can obtain the helix shaft's actual speed within 6.4 microseconds. The shaft register is loaded with the shaft counter's value when the *System _0_Index pulse is received. Thus, the shaft count is available to be read by the computer for one complete shaft revolution. The shaft register is cleared immediately after the computer has read the register contents.

The computer can determine if the shaft is rotating very slowly or not at all by sampling the shaft register two times in succession. The first shaft sample reads the shaft register then clears the register. A second shaft sample is executed after waiting an appropriate time interval for approximately one shaft revolution to occur. If a zero value is received, the shaft is rotating very slowly or not at all.

4.7. COMPUTER INTERRUPT REQUEST

Normally, an interrupt request IRQ10 is sent to the computer whenever the *System_0_ Index pulse is received from the double helix shaft sensors. This informs the computer when the helix shaft is at 0 degree for a reference point. An interrupt request IRQ11 is also sent to the computer whenever the *System_180_Index is received. A third interrupt, called Page_INT, is available as IRQ15. It can be programmed to generate a Page Interrupt whenever the display has read out a Page of Data (programmable, nominally set at 4K or 8K data points).

4.8. MULTIPLE COLOR/MULTIPLE COMPUTER SYNCHRONIZATION

Multiple color/multiple computer configuration, figure 3-6a, shows the basic cable hookup to synchronize three volumetric boards where one of the boards is in another computer. Each board handles the control of a different colored laser beam in this system. Figure3-6b lists additional multiple color/ multiple computer synchronization cabling details.

The volumetric board that drives the green laser is programmed to be the Master in figure 3-6a. This means the source of the system's 20-MHz clock will be the 20-MHz crystal oscillator on the card designated GREEN. The other cards (RED, BLUE, etc.) will be programmed as slaves.

They receive the master's system 20-MHz clock and use this for their internal 20-MHz clock instead of their own crystal oscillator to keep in synchronization. This circuitry synchronizes additional volumetric cards in a single computer or multiple computers to within the master board's clock period of 1/20 MHz or 50 nanoseconds, if the external cables are short.

When two or more computers are used, the volumetric cards in the slave computer must also synchronize all of their internal clocks to the master's internal clock. This is accomplished when the slave computer receives the *SYS_RESET signal, which clears counter "C", thereby resetting all the internal clocks on the volumetric cards to match the master clock. See figure 3-7.

Figure 3-7 shows the internal system 20-MHz clock circuitry when the board has been selected as the Master. The 20-MHz signal is buffered and sent to the rest of the system, as well as being used internally.

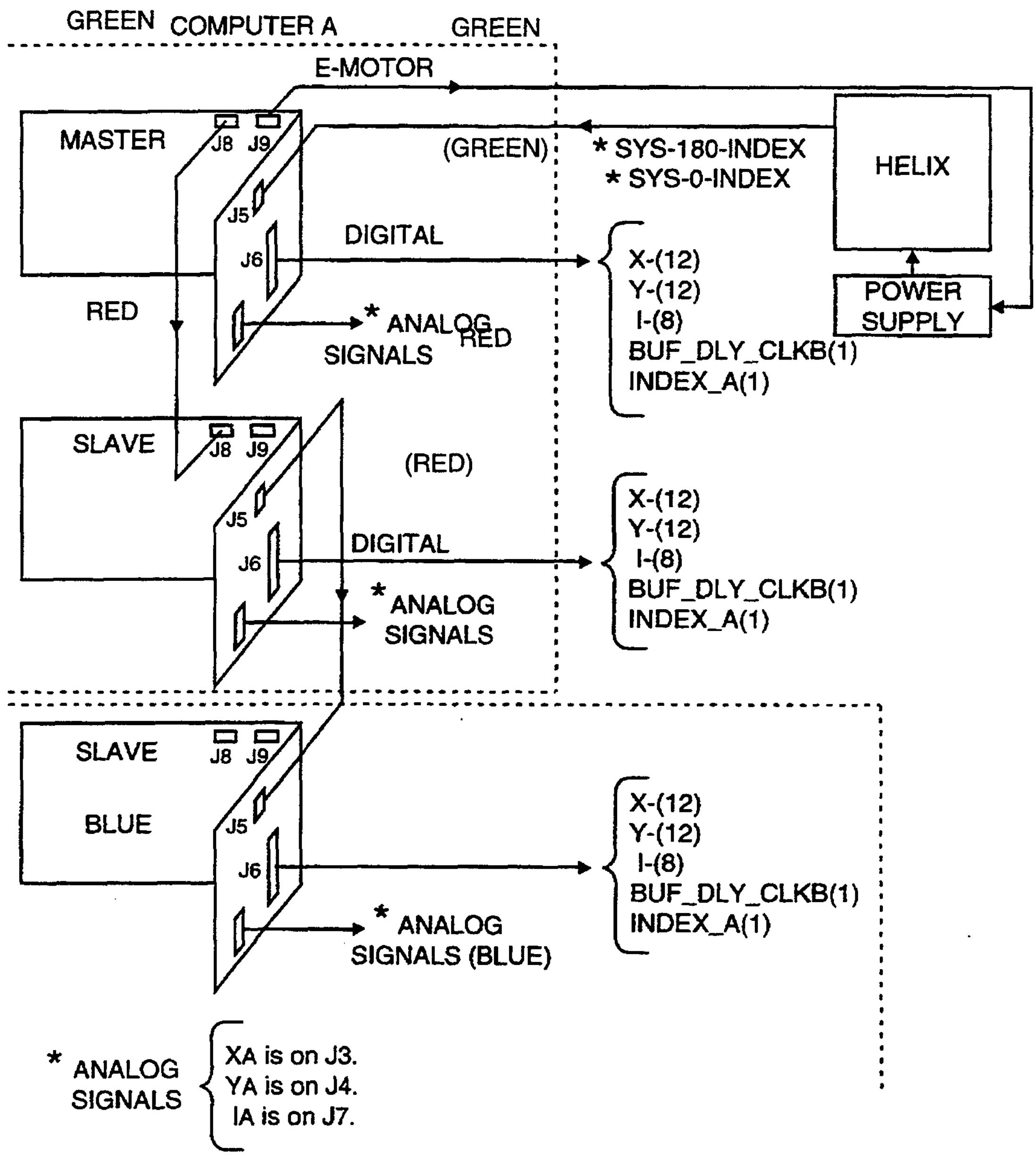


Figure 3-6a. Multiple color/multiple computer configuration.

```
J8 MASTER BOARD TO J8 SLAVE BOARD (1:1)
        1     SYS_20MHZ        1
        2     DGND             2
        3     N/C              3
        4     *SYS_RESET       4
        5     *SYS_0_INDEX     5
        6     *SYS_180_INDEX   6

J5 SLAVE BOARD TO J5 SLAVE BOARD (1:1)
        1     SYS_20MHZ#1      1
        2     DGND             2
        3     N/C              3
        4     *SYS_RESET#1     4
        5     *SYS_0_INDEX     5
        6     *SYS_180_INDEX   6

J5 MASTER BOARD FROM HELIX POSITION SENSORS
        1     N/C (P16 JUMPER OPEN)
        2     DGND
        3     N/C
        4     N/C (P17 JUMPER OPEN)
        5     *SYS_0_INDEX (INPUT FROM HELIX SENSOR)
        6     *SYS_180_INDEX (INPUT FROM HELIX SENSOR)

J9 MASTER BOARD TO HELIX MOTOR POWER SUPPLY
        1     AGND
        2     E_MOTOR


GREEN     1. Set System Master Bit HIGH in "PARAMETER REGISTER"
MASTER    2.   No Jumper on P16.
               No Jumper on P17.
               Jumper:    P31-1 to P31-2  PAGE_INT FF to IRQ15_AT.
                          P35-1 to P35-2  INT_180 FF to IRQ11_AT.
                          P36-1 to P36-2  INT_0 FF to IRQ10_AT.

RED       1.   Clear System Master Bit in "PARAMETER  REGISTER".
SLAVE     2.   Jumper:    P16-1 to P16-2.
                          P17-1 to P17-2.

BLUE      1.   Clear System Master Bit in "PARAMETER  REGISTER".
SLAVE     2.   Jumper:    P16-1 to P16-2.
                          P17-1 to P17-2.
```

Note: See additional jumpers required as listed in section 2.

Figure 3-6b. Multiple color/multiple computer cabling details.

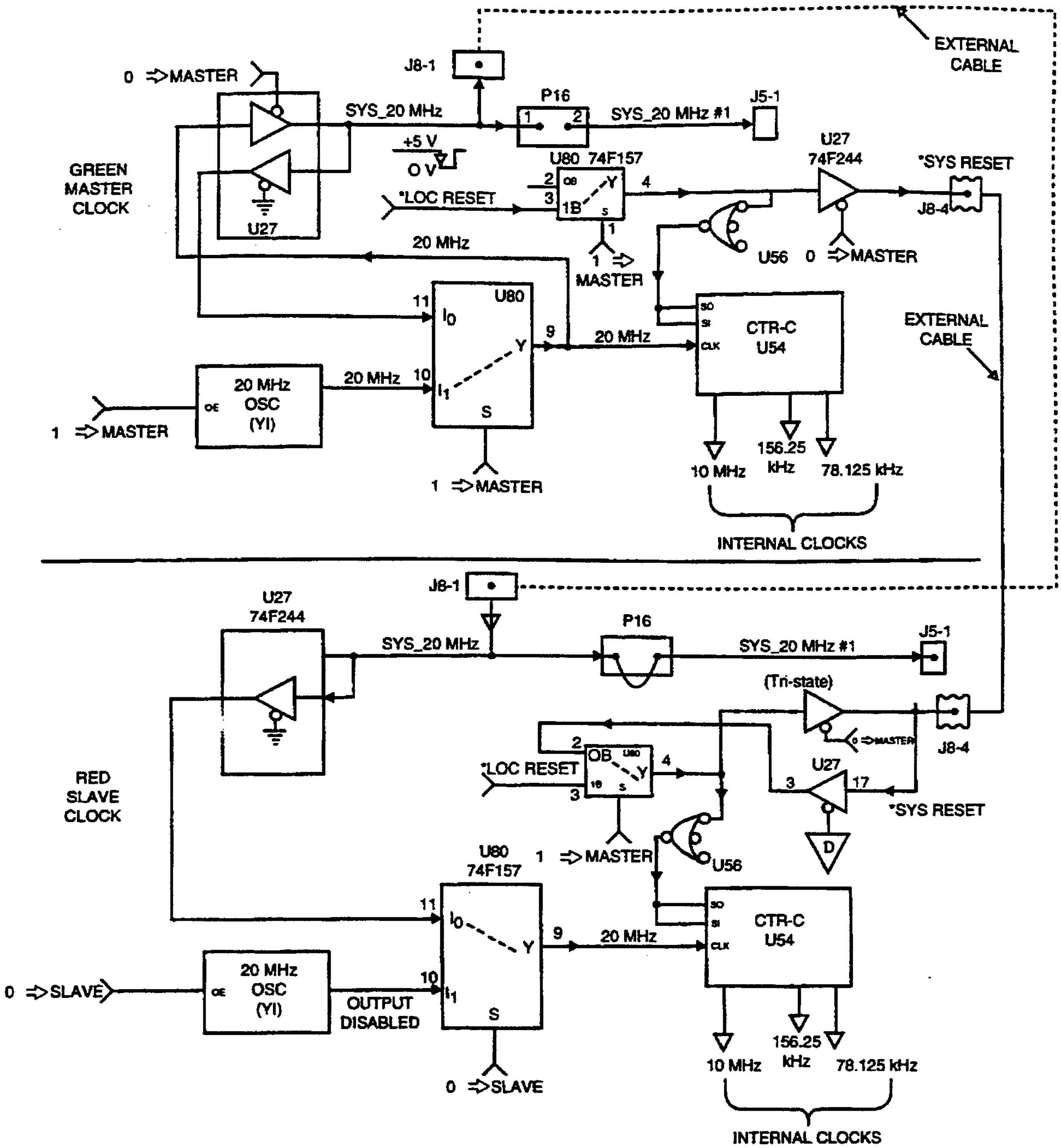


Figure 3-7. Internal system 20-MHz clock and *SYS_RESET circuitry for GREEN master and RED slave cards.

Table 3-1. SSC San Diego J6 connector pinouts.

SSC SD Conn.	Term	SSC SD Conn.	Term
J6–1	BUFF DLY CLKB	J6–27	ID7 (MSB Intensity)
		J6–28	ID6
J6–2	Digital Grd	J6–29	ID5
		J6–30	ID4
		J6–31	ID3
J6–3	XO0 (LSB) X Output	J6–32	ID2
J6–4	XO1	J6–33	ID1
J6–5	XO2	J6–34	ID0 (LSB Intensity)
J6–6	XO3		
J6–7	XO4	J6–35	Digital GRD
J6–8	XO5		
J6–9	XO6	J6–36	INDEX A
J6–10	XO7		
J6–11	XO8		
J6–12	XO9		
J6–13	XO10		
J6–14	XO11 (MSB) X Output		
J6–15	YO0 (LSB) Y Output		
J6–16	YO1		
J6–17	YO2		
J6–18	YO3		
J6–19	YO4		
J6–20	YO5		
J6–21	YO6		
J6–22	YO7		
J6–23	YO8		
J6–24	YO9		
J6–25	YO10		
J6–26	YO11 (MSB) Y Output		

4.9. SUMMARY OF MAJOR VOLUMETRIC #2 BOARD FUNCTIONS

a. The present board has a dual-port RAM memory that holds up to 65,536—32-bit- wide words. Each word defines a point that has 12 bits for X and 12 bits for Y, and 8 bits of intensity. The MSB of digital X11 and Y11 are used for analog intensity control as Extended Video and Full Width Video, respectively.

   The 12 bits of X and Y are read from port "B" of the dual-port RAM and then sent to the Newport Electro-Optics System's 40K scanner interface board. The NEOS board drives separate X and Y RF synthesizers for the NEOS acousto-optic laser deflection circuitry.

b. The motor speed control regulates the speed of the 3-D display's shaft since it sends a 16-bit word to the motor register, where the lower 12 bits of it are converted by a 12-bit DAC to furnish a nominal 0 V to +10 V control signal to the helix dc motor power supply.

c. The shaft's speed circuitry accurately determines the helix shaft's actual speed within 6.4 microseconds (156.25-kHz clock) by counting the clocks between two *System_0 Index pulses. The *System_0 Index pulse occurs whenever the shaft reaches 0 degree.

d. Multiple color/multiple computer sync circuitry synchronizes additional volumetric cards in a single computer or multiple computers to within the master board's clock period of 1/20 MHz or 50 nanoseconds.

e. Intensity circuitry controls the amplitude and PW of the output video on a voxel-by-voxel basis. The video intensity signal is available to the acousto-optic modulator as a gated analog voltage (0 to +1 V max into 50 ohms at J7) as well as an 8-bit transistor-transistor logic (TTL) digital signal at J6.

f. The above functions are implemented in an 10-layered printed circuit board that is designed to fit into a standard IBM computer expansion Industry Standard Architecture (ISA) slot. The board has a component count of 448 items with a mixture of surface mount and discrete components.

4.10. ADVANTAGES OF DUAL-PORT MEMORY

The dual-port memory allows the port "B" readout timing of each addressed point to be *independent* of the computer software instruction execution FLOW, such as adding or deleting instructions, processing an interrupt, accessing the disk, etc.

Once the dual-port RAM has been loaded via port "A" with image points, the common memory image is continuously readout via port B at the designated refresh rate without using the computer or *any ISA bus bandwidth.* The volumetric card allows a PC with a standard expansion ISA slot to accurately control the position of a single laser on a 3-D display.

Multiple lasers require additional volumetric cards (one per laser beam) that can be located in the same computer or in another computer and can be run synchronously or asynchronously. Each card can add another 38,461 voxels at a 20-Hz refresh rate to the display with CTR0 = 13.

5. VOLUMETRIC #2 COMMANDS AND JUMPER OPTIONS

Direct Memory Mapping is used to read and write 16-bit words to or from volumetric #2's Memory "A" (MEMA). Memory "A" can hold 65,536—32-bit volumetric words or a block of 262,144 bytes.

5.1. DIRECT MEMORY MAPPED BASE ADDRESS (MBA) IN BYTES

MBA = 0C 0000 hex + N (04 0000) hex

where N = 0 to 60 dec (3C) hex.

Note: The "IBM AT" Address Bus has a total of 24 address lines.

Normally, the value N = 0 is not used since EGA BIOS, VGA BIOS, and RAM BIOS, etc., memory addresses are in this 0C 0000 hex to 0F FFFF hex area for both the Diversified Technology (486-DX2-50 MHz) and the UNISYS PW 820 COP (386/20 MHz) computers.

6. DIRECT MEMORY MAPPED TEST POINTS

*P1 EQ Q1	TP14–6	SW3 settings match Direct Memory Mapped address when active low.
*AT Data Bus En	TP18–9	Activates 16-bit Data Buffers to/from AT Bus when active low.
*LD ML Reg	TP14–10	Load MEMA lower 16 bits into ML Reg.
*LD MEMA (32 bits)	TP14–9	Write 32 bits into MEMA (lower 16 bits from ML Register).
*RD MEMA UPPER	TP14–8	Read MEMA upper 16 bits (M31–M16).
	TP14–7	Read MEMA lower 16 bits (M15–M0).

Experiments using the Compaq 386-33 computer allowed Direct Memory Mapped data to be written to the "AT" bus. Whenever the memory address exceeded the internal memory (12 MB in this case), the data would go to or from the "AT" bus. Thus, on this machine, addresses of 12 MB (C0 0000 hex) through 16 MB (FF FFFF hex) are Direct Memory Mapped to the "AT" bus with the current internal 12 MB of RAM.

The Compaq 386-25 computer allows Direct Memory Mapped addresses from 12 MB through 16 MB to go directly to the "AT" bus when the cache memory switch SW1-3 is disabled. Since it is not known exactly how the Diversified Technology (486-DX2-50) or the UNISYS PW 820 COP (386/20) computers are configured, we will initially select the Direct Memory Base address to be C0 0000 hex or 12,582,912 decimal.

Memory "A" address 0000 hex (lower 16 bits) is at Direct Memory Base address plus zero. Memory "A" address 0000 hex (upper 16 bits) is at Direct Memory Base address plus 2.

7. MEMORY “B” INFORMATION FORMAT

	2nd 16-Bit Wd (Upper)		lst 16-Bit Wd (Lower)	
Mem “B”	M31------M20	M19--M16	M15-----M08	M07------M00
Data Bus	D15------D04	D03--D00	D15-----D08	D07------D00
Terms	X11------X00	Y11--Y08	Y07-----Y00	I07------I00
	(MSB)----(LSB)	(MSB)	(LSB)	(MSB)----(LSB)

Notes: X11 bit is X11 or Extended Video depending on whether the *Digital* or *Analog* Mode is used. Y11 bit is Y11 or Full Width Video depending on whether the *Digital* or *Analog* Mode is used.

The Input/Output Memory address (I/O address) allows commands such as Read X-DAC Table, Load X-DAC Table, etc., to be decoded.

The I/O Address consists of a four-digit *Hex number* defined as follows:

I/O Address = [Main I/O 16 Bit Base Address + Index #1] + Index #2

where SW1 and SW2 switch settings determine the I/O address.

Main I/O Mapped 16-bit Base Address = XX00 hex.
Index #1 hex = 00, 40, 80, or C0.
Index #2 hex = 0X, 1X, or 2X. (See following table).

Example: Load CTRB INITIAL Reg with I/O Base address = B100 hex and Index #1 = 40 hex. Index #2 is 10 hex from the following table.

The resulting I/O address is B150 hex.

Index #2 (hex)	16-Bit I/O Commands	Active Low
00 Rd	Read ML Reg.	U69–15 (TP13–2)
00 Wr	(Spare).	U67–15 (TP12–2)
02 Rd	(Spare).	U69–14 (TP13–3)
02 Wr	(Spare).	U67–14 (TP12–3)
04 Rd	(Spare).	U69–13 (TP13–4)
04 Wr	(Spare).	U67–13 (TP12–4)
06 Rd	Read X-DAC Table.	U69–12 (TP13–5)
06 Wr	Load X-DAC Table.	U67–12 (TP12–5)
08 Rd	Read Y-DAC Table.	U69–11 (TP13–6)
08 Wr	Load Y-DAC Table.	U67–11 (TP12–6)
0A Rd	Read Shaft Reg then clear.	U69–10 (TP13–7)
0A Wr	Load Motor Speed Register (D11 through D0).	U67–10 (TP12–7)
0C Rd	Read LUT Data Inc Add.	U69–9 (TP13–8)
0C Wr	Load LUT Data Inc Add.	U67–9 (TP12–8)
0E Rd	Read Counter “B.”	U69–7 (TP13–9)
0E Wr	Generate local reset.	U67–7 (TP12–9)

Index #2 (hex)	16-Bit I/O Commands	Active Low
10 Rd 10 Wr	(Spare). Load CTRB INITIAL reg.	U70–15 (TP11–2) U78–15 (TP15–2)
12 Rd 12 Wr	(Spare). Generate test CLKB.	U70–14 (TP11–3) U78–14 (TP15–3)
14 Rd 14 Wr	(Spare). Load LUT CTR (8 LSBs).	U70–13 (TP11–4) U78–13 (TP15–4)
16 Rd 16 Wr	(Spare). Load LUT Page Reg. (MSG's) [D10, D9, D8]	U70–12 (TP11–5) U78–12 (TP15–5)
18 Rd 18 Wr	(Spare). Load LUT DISPLAY PG Reg. (MSB's) [D2, D1, D0].	U70–11 (TP11–6) U78–11 (TP15–6)
1A Rd 1A Wr	Clear 0 Degree Interrupt. Load Parameter Reg. D0 EN_CTR0_1. D1 EN_CTR2. D2 SYSTEM_MASTER. D3 INTO_EN. D4 INT1_EN. D5 PG_INT_EN.	U70–10 (TP11–7) U78–10 (TP15–7)
1C Rd 1C Wr	Clear 180 Degree Interrupt. (Spare).	U70–9 (TP11–8) U78–9 (TP15–8)
1E Rd 1E Wr	Clear Page Interrupt. (Spare).	U70–7 (TP11–9) U78–7 (TP15–9)

Index #2 (hex)	8-Bit I/O Commands	Active Low
20 R/W	82C54 CTR0 CS	U24–15 (TP5–2)
21 R/W	82C54 CTR1 CS	U24–14 (TP5–3)
22 R/W	82C54 CTR2 CS	U24–13 (TP5–4)
23 R/W	82C54 CW CS	U24–12 (TP5–5)
24 W	Sel CTRB CT DOWN	U24–11 (TP5–6)
25 W	Sel CTRB CT UP	U24–10 (TP5–7)
26 R/W	SPARE	U24–9 (TP5–8)
27 R/W	SPARE	U24–7 (TP5–9)

8. VOLUMETRIC #2 JUMPERS

Ref #__	Board Location	Schematic Location	Description
P3	1DD4	6D3	P3– 1 X(8) source. P3–2 X(8) to X-DAC EEPROMs address. P3–3 Digital ground.
P4	1DD4	6D4	P4–1 X(11) MSB source. P4–2 X(11) MSB to X-DAC EEPROMS address. P4–3 Digital ground.
P5	1DD4	6D4	P5–1 X(9) source. P5–2 X(9) to X-DAC EEPROMS address. P5–3 Digital ground.
P6	1DD4	6D4	P6–1 X(10) source. P6–2 X(10) to X-DAC EEPROMS address. P6–3 Digital ground.
P7	1DD4	6A5	P7–1 Enbl LUT Data to Data Bus (20-ns Dly). P7–2 Enbl LUT Data to Data Bus pin on U30. P7–3 Enbl LUT Data to Data Bus (10-ns Dly).
P8	1DD4	7A8	P8–1 Digital ground. P8–2 Extended Video control. P8–3 Extended Video bit (source).
P9	1DD4	6B3	P9–1 Y(8) source. P9–2 Y(8) to Y-DAC EEPROM's address. P9–3 Digital ground.
P10	1DD4	6B4	P10–1 Y(9) source. P10–2 Y(9) to Y-DAC EEPROM's address. P10–3 Digital ground.
P11	1DD3	2E4	P11–1 System 20-MHz Clock. P11–2 Digital ground.
P12	1CC3	2F5	P12–1 *System Reset. P12–2 Digital ground.
P13	1AA7	2B3	P13–1 *Sync 180 Degree Index. P13–2 Int 0 Flip Flop (U132) preset. P13–3 *Sync 0 Degree Index. P13–4 *Sync 180 and *Sync 0 Index.
P14	1DD1	2C1	P14–1 E-Motor R49 (10 ohm) bypass. P14–2 E-Motor R49 (10 ohm) bypass.
P15	1DD1	2C1	P15–1 E-Motor analog voltage. P15–2 Analog ground.
P16	1DD1	2E4	P16–1 System 20 MHz. P16–2 System 20 MHz #1 to J5–1.
P17	1CC1	2F4	P17–1 *System Reset. P17–2 *System Reset #1.

Ref #__	Board Location	Schematic Location	Description
P18	1CC6	6B4	P18–1 Y(10) source. P18–2 Y(10) to Y-DAC EEPROM's address. P18–3 Digital ground.
P19	1CC6	3F5	P19–1 *P1 EQ Q1. P19–2 *P1 EQ Q1 SW (Address A Buffer Enable). P19–3 Digital ground.
P20	1BB6	2E5	P20–1 Jumper if local reset active in Slave Mode. Allows local reset to Clr CtrC. P20–2 *Local reset.
P21	1BB8	2D4	P21–1 625-kHz clock. P21–2 Shaft Counter clock line. P21–3 312.5-kHz clock. P21–4 156.25-kHz clock.
P22	1AA8	1C7	P22–1 Jumper for *Sync 180 Index to resync and reload 82C54 counters 0 and 1. Connects to U25–2. P22–2 *Sync 180 Index.
P23	1AA8	1C2	P23–1 *Sync 180 Index. P23–2 Int 180 Flip Flop (U51) Preset. P23–3 *Sync 0 Index. P23–4 *Sync 180 Index and *Sync 0 Index.
P24	1AA7	2C3	P24–1 *Sync 180 Index. P24–2 Ct Down Flip Flop (U132) clear pin. P24–3 *Sync 0 Index.
P25	1AA7	2D3	P25–1 *Sync 180 Index. P25–2 Ct Down Flip Flop (U132) preset pin. P25–3 *Sync 0 Index. P25–4 Ctr "B" S1 line.
P26	1AA7	2C3	P26–1 *CLR. P26–2 *Sync 180 Index. P26–3 *Sync 0 Index. P26–4 *Sync 180 and *Sync 0 Index. P26–5 *Sync 180 and *Sync 0 Index. P26–6 Ctr "B" S0 line.
P27	1AA6	3E8	P27–1 Digital ground. P27–2 Continuous enable of Dly ClkB ColX.
P28	1BB6	2B2	P28–1 *Sync 180 Index. P28–2 *Load, Clrs CtrB S0 and ClkB items. P28–3 *Sync 0 Index.
P29	1AA5	7B6	P29–1 Digital ground. P29–2 Full Width Video Control. P29–3 Full Width Video.

Ref #__	Board Location	Schematic Location		Description
P30	1AA5	7A6	P30–1	Digital ground.
			P30–2	Page Count Control.
			P30–3	Page Count Complete.
P31	1AA5	1C3	P31–1	IRQ15-AT.
			P31–2	Page Interrupt Source.
P32	1BB5	6B4	P32–1	Y(11) MSB Source.
			P32–2	Y(11) MSB to Y-DAC EEPROM's address.
			P32–3	Digital ground.
P33	1AA4	6F6	P33–1	ClkB.
			P33–2	ClkB delayed 140 ns.
			P33–3	Dly ClkB Source.
			P33–4	ClkB delayed 175 ns.
P34	1AA5	2B2	P34–1	DW Sync 0 or 180 Index.
			P34–2	AND Gate U75 Input to ClkB.
			P34–3	Double Wide (DW) Sync 180 Index.
			P34–4	DW Sync 0 Index.
			P34–5	Input to U141 gate to ClkB.
			P34–6	Digital ground.
			P34–7	*Test ClkB.
P35	1AA3	1C1	P35–1	IRQ11_AT.
			P35–2	Int 180 source.
P36	1AA2	2A1	P36–1	IRQ10_AT.
			P36–2	INT0.
			P36–3	Spare.
P37	1DD3	2F5	P37–1	100K-ohm pullup to +5 V.
			P37–2	*System Reset.
E1	1DD2	2F8	E1–1	*Sys 180 Index Input.
			E1–2	Digital ground.
E2	1DD2	2E8	E2–1	*Sys 0 Index Input.
			E2–2	Digital ground.
E3	1CC1	7E2	E3–1	Y Analog Output 50-ohm resistor shorting terminal.
			E3–2	Y Analog Output 50-ohm resistor shorting terminal.
E4	1CC1	7D2	E4–1	Y Analog Output.
			E4–2	Analog ground.
E5	1CC1	7F2	E5–1	X Analog Output 50-ohm resistor shorting terminal.
			E5–2	X Analog Output 50-ohm resistor shorting terminal.
E6	1CC1	7F2	E6–1	X Analog Output.
			E6–2	Analog ground.
E7	1AA8	2D4	E7–1	5-MHz Clock.

Ref #__	Board Location	Schematic Location		Description
E8	1AA8	2D4	E8–1	2.5-MHz Clock.
E9	1AA8	2D4	E9–1	1.25-MHz Clock.
E10	1AA8	2D4	E10–1	78.125-kHz Clock.
E11	1AA8	2D4	E11–1	625-kHz Clock.
E12	1AA8	2D4	E12–1	312.5-kHz Clock.
E13	1AA8	2D4	E13–1	156.25-kHz Clock.
E14	1BB5	3A5	E14–1	*RCO of CtrB.
E15	1AA1	7C1	E15–1	Ia Analog Intensity.
			E15–2	Analog ground.

9. VOLUMETRIC #2 JUMPERS (NOMINAL SETTINGS FOR GREEN MASTER 40K SCANNER)

P3–1 to P3–2	X(8) Source to X-DAC EEPROMS A8 address bit.
P4–1 to P4–2	X(11) MSB Source to X-DAC EEPROMS A11 address bit.
P5–1 to P5–2	X(9) Source to X-DAC EEPROMs A9 address bit.
P6–1 to P6–2	X(10) Source to X-DAC EEPROMs A10 address bit.
P7–2 to P7–3	Enbl LUT Data to Data Bus 10-ns Dly to U30-19 Gate. **Note:** Board also seems to work correctly with 20-ns Dly option.
P8–2 to P8–3	Extended Video X11 Bit (Source) jumpered to Extended Video Control signal (optional). Jumper only affects the Analog Intensity output which is not used in the NEOS 40K scanner.
P9–1 to P9–2	Y(8) Source to Y-DAC EEPROMs A8 address bit.
P10–1 to P10–2	Y(9) Source to Y-DAC EEPROMs A9 address bit.
P13–2 to P13–3	*Sync 0 Degree Index jumpered to Int 0 Flip Flop (U132) Preset pin. Sets INT0 Flip Flop and generates the 0-degree computer interrupt every time the helix shaft position reaches 0 degree as indicated when the *Sync 0 Index signal goes active (low).
P18–1 to P18–2	Y(10) Source to Y-DAC EEPROMs A10 address bit.
P19–2 to P19–3	Jumper *P1 EQ Q1 SW term (Address A Buffer Enbl) to Digital ground. Continuously Enables 74ALS244 Address “A” Buffers.
P21–2 to P21–4	Select 156.25-kHz Clock for Shaft Counter Clock Line.
P22–1 to P22–2	*Sync 180 Index signal jumpered to U25-2 to resync and reload 82C54 counters 0 and 1.
P23–1 to P23–2	*Sync_180_Index jumpered to Int 180 Flip Flop (U51) Preset pin. Sets INT_180 Flip Flop and generates the 180-degree computer interrupt every time the helix shaft position reaches 180 degrees as indicated when the *Sync_180 signal goes active (low).
P26–4 to P28–2	*Sync_0_Index or *Sync_180_Index will, respectively, generate a 100-ns active low pulse on CTR B-S0 and an active 100-ns low pulse on ClkB. This parallel loads CTR B with the contents of the Initial Register.
P27–1 to P27–2	Continuous Enable of Dly_ClkB Column X.
P30–1 to P30–2	Page Count Control jumpered to digital ground. Bypasses PG_CNT_Complete signal from the Analog Intensity logic.
P31–1 to P31–2	IRQ15_AT Computer Interrupt from PAGE_INT Flip Flop. Counter 1 of the N82C54-2 IC Timer sets this Interrupt (**Master Card Only**).
P32–1 to P32–2	Y(11) MSB Source to Y-DAC EEPROMs A11 address bit.
P35–1 to P35–2	IRQ11_AT Computer Interrupt from INT_180 Flip Flop (**Master Card Only**).
P36–1 to P36–2	IRQ10_AT Computer Interrupt from INT0 Flip Flop (**Master Card Only**).

10. VOLUMETRIC #2 SWITCH POSITIONS FOR GREEN NEOS 40K SCANNER

The Direct Memory Mapped Base Address is chosen as: MBA = C0 0000 (hex). This allows a 256-KByte block of memory addresses beginning at C0 0000 to be directly mapped into Channel A of the dual-port memory.

```
Set SW3 to      hex          C         0         0     0     0     0
C0 0000 hex:    binary    1 1 0 0   0 0 0 0   xxxx  xxxx  xxxx  xxxx *
                SW3 #     1 2 3 4   5 6 7 8

                          O O O O   O O O O
                          F F N N   N N N N
                          F F
```

*Decoded elsewhere.

The Input/Output Memory Address (I/O address) is chosen as 0240 (hex) for the Green 40K Scanner. This allows commands such as Read X-DAC Table, Load X-DAC Table, etc., to be decoded.

```
                                /------SW1------\      /-SW2-\
Set SW1 and SW2      hex           0        2           4        0
to 0240 hex:         binary     0 0 0 0  0 0 1 0     0 1 xx   xxxx *
                    SWposition  1 2 3 4  5 6 7 8     1 2

                                O O O O  O O O O     O O
                                N N N N  N N F N     N F
                                             F         F
```

*Decoded elsewhere.

Note: The volumetric #2 card driving the GREEN 40K Scanner should be configured as MASTER. (See Parameter Reg, System Master Bit D2 = 1.) See p. 19.

11. MASTER CARD REQUIRED JUMPER SETTINGS

P36–1 to P36–2	IRQ10_AT Computer Interrupt from INT0 Flip Flop (**Master Card Only**).
P35–1 to P35–2	IRQ11_AT Computer Interrupt from INT_180 Flip Flop (**Master Card Only**).
P31–1 to P31–2 (Optional)	IRQ15_AT Computer Interrupt from PAGE_INT Flip Flop. Counter 1 of the N82C54-2 IC Timer sets this Interrupt. (Optional Jumper)

12. VOLUMETRIC #2 SWITCH POSITIONS FOR RED NEOS 40K SCANNER

The Direct Memory Mapped Base Address is chosen as: MBA = C4 0000 (hex). This allows a 256-KByte block of memory addresses beginning at C4 0000 to be directly mapped into Channel A of the dual port memory.

```
Set SW3 to      hex          C          4        0     0     0     0
C4 0000 hex:    binary    1 1 0 0    0 1 0 0    xxxx  xxxx  xxxx  xxxx *
                SW3#      1 2 3 4    5 6 7 8

                          O O O O    O O O O
                          F F N N    N F N N
                          F F          F
```

*Decoded elsewhere.

The Input/Output Memory Address (I/O address) is chosen as 0340 (hex). This allows commands such as Read X-DAC Table, Load X-DAC Table, etc., to be decoded.

```
                                 /------SW1------\       /-SW2-\
Set SW1 and SW2    hex              0          3           4        0
to 0340 hex:       binary        0 0 0 0    0 0 1 1      0 1 xx   xxxx *
                 SWposition      1 2 3 4    5 6 7 8      1 2

                                 O O O O    O O O O      O O
                                 N N N N    N N F F      N F
                                                F F        F
```

*Decoded elsewhere.

Note: The volumetric #2 card driving the RED 40K Scanner should be configured as a SLAVE (See Parameter Reg, System Master Bit D2 = 0.)

13. VOLUMETRIC #2 JUMPERS (NOMINAL SETTINGS FOR RED SLAVE 40K SCANNER)

P3–1 to P3–2	X(8) Source to X-DAC EEPROMs A8 address bit.
P4–1 to P4–2	X(11) Source to X-DAC EEPROMs A11 address bit.
P5–1 to P5–2	X(9) Source to X-DAC EEPROMs A9 address bit.
P6–1 to P6–2	X(10) Source to X-DAC EEPROMs A10 address bit.
P7–1 to P7–3	Enbl LUT Data to Data Bus 10-ns Dly to U30-19 Gate. Note: Board also seems to work correctly with 20-ns Dly option.
P8–2 to P8–3	Extended Video X11 Bit (Source) jumpered to Extended Video Control signal (optional). Jumper only affects the Analog Intensity output which is not used in the NEOS 40K scanner.
P9–1 to P9–2	Y(8) Source to Y-DAC EEPROMs A8 address bit.
P10–1 to P10–2	Y(9) Source to Y-DAC EEPROMs A9 address bit.
P13–2 to P13–3	*Sync 0 Degree Index jumpered to INT0 Flip Flop (U132) Preset pin. Sets INT0 Flip Flop and generates the 0-degree computer interrupt every time the helix shaft position reaches 0 degree as indicated when the *Sync 0 Index signal goes active (low).
P18–1 to P18–2	Y(10) Source to Y-DAC EEPROMs A10 address bit.
P19–2 to P19–3	Jumper *P1 EQ Q1 SW term (Address A Buffer Enbl) to Digital ground. Continuously enables 74ALS244 Address “A” Buffers.
P21–2 to P21–4	Select 156.25 kHz Clock for Shaft Counter Clock Line.
P22–1 to P22–2	*Sync 180 Index signal jumpered to U25-2 to resync and reload 82C54 counters 0 and 1.
P23–1 to P23–2	*Sync_180_Index jumpered to Int 180 Flip Flop (U51) Preset pin. Sets INT_180 Flip Flop and generates the 180-degree computer interrupt every time the helix shaft position reaches 180 degrees as indicated when the *Sync_180 signal goes active (low).
P26–4 to P28–2	*Sync_0_Index or *Sync_180_Index will, respectively, generate a 100-ns active low pulse on CTR B-S0 and an active 100-ns low pulse on ClkB. This parallel loads CTR B with the contents of the Initial Register.
P27–1 to P27–2	Continuous enable of Dly_ClkB Column X.
P30–1 to P30–2	Page Count Control jumpered to digital ground. Bypasses PG_CNT_Complete signal from the Analog Intensity logic.
P31–1 to P31–2 (Optional)	IRQ15_AT Computer Interrupt from PAGE_INT Flip Flop. Counter 1 of the N82C54-2 IC Timer sets this Interrupt. (Optional Jumper).
P32–1 to P32–2	Y(11) MSB Source to Y-DAC EEPROMs A11 address bit.
P35–1 to P35–2 (Open)	IRQ11_AT Computer Interrupt from INT_180 Flip Flop disabled.
P36–1 to P36–2 (Open)	IRQ10_AT Computer Interrupt from INT0 Flip Flop disabled.

14. SPECIAL SIGNALS

Special Signals	Source	Destinations
*Sys_0_Index.	External	E2–1, U46–1, J5–5, J8–5.
*Sync_0_Index.	U59–11	P13–3, P23–3, P24–3, P25–3, P26–3, P28–3, U59–10, U119–14 and 23, U127–14 and 23, U131–12.
DW_Sync_0_Index.	U58–11	P34–4, U58–1 and 2, U75–5, U125–11 and 23.
*Sys_180_Index.	External	E1–1, U46–3, J5–6, J8–6.
*Sync_180_Index.	U59–3	P13–1, P22–2, P23–1, P24–1, P25–1, P26–2, P28–1, U131–13.
DW_Sync_180_Index.	U58–8	P34–3, U75–4.
*Sync_180_and *Sync_180_Index.	U131–11	P13–4, P23–4, P26–4, P26–5.
DW_Sync_0_or_180_Index.	U75–6	P34–1.
*IOR	U95–14	TP19–10, U28–26, U68–1, U69–5, U70–5.
*IOW	U95–12	TP19–9, U28–27, U68–2, U68–5, U67–4, U78–5.

15. VOLUMETRIC #2 PARTS LIST INFORMATION

The volumetric #2 parts are listed by a designator number (Uxx, Rxx, Yxx, Cxx, TPxx, Pxx, SWxx, Jxx, VRxx, etc.). Each designator entry describes the item, its part number, schematic location (sheet and zone), and the physical board location of that part. Power and ground pins are also listed if applicable.

Item U1 is listed at board location 1DD9, where the initial number 1 is Layer 1 (Top Layer) at location DD9 (Row DD, Column 9) on the layout drawing. If the board location was on the back (Layer 10), the board location would have been 10DD9.

The schematic entry of 4B7 indicated that this part is shown on sheet 4 of the schematics at zone B7.

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U1	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns (68-pin PLCC)	1DD9	4B7	+5 V Gnd	17,22,6 8 14,18,3 5, 52
U2	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1DD8	4B6		
U3	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1DD8	4E7		
U4	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1DD7	4E6	+5 V Gnd	17,12,6 8 14,18,3 5, 52
U5	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1CC9	4B5		
U6	IDT 7006S35J, 16K X 8 dual-port RAM, 35 ns	1CC8	4B4		
U7	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1CC8	4E5		
U8	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	1CC7	4E4	+5 V Gnd	17,22,6 8 14,18,3 5, 52
U9	SEEQ LQ28HC32–55, 4K x 8, 55-ns EEPROM, (32-pin LCC)	1DD5	6E2	+5 V Gnd	32 16
U10	SEEQ LQ28HC32–55, 4K x 8, 55 ns EEPROM	1CC5	6F2		

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U11	SEEQ LQ28HC32–55, 4K x 8, 55-ns EEPROM	1CC5	6B2		
U12	SEEQ LQ28HC32–55, 4K x 8, 55-ns EEPROM	1BB5	6C2	+5 V Gnd	32 16
U13	74ALS245ADW TI octal bus XFR	1DD5	6B1	+5 V Gnd	20 10
U14	74F244DW TI octal bus DVR	1CC5	6C4	+5 V Gnd	20 10
U15	IDT 6116SA25Y, 2K x 8, 25-ns RAM	1CC5	6C6	+5 V Gnd	24 12
U16	74ALS244BDW TI octal bus DVR	1BB5	3D4	+5 V Gnd	20 10
U17	74ALS174D TI hex D FF	1DD5	6C7	+5 V Gnd	16 8
U18	74ALS245ADW TI octal bus XFR	1CC5	6E1	+5 V Gnd	20 10
U19	74ALS245ADW TI octal bus XFR	1CC5	6C1	+5 V Gnd	20 10
U20	74ALS244BDW TI octal bus DVR	1BB5	1E3	+5 V Gnd	20 10
U21	74F157AD 2:1 MUX	1DD5	6C7	+5 V Gnd	16 8
U22	74F574DW octal D FF	1CC4	6D5	+5 V Gnd	20 10
U23	74ALS874BDW octal D FF	1CC4	2E3	+5 V Gnd	24 12
U24	74F138D 3 to 8 decoder	1BB4	1D4	+5 V Gnd	16 8
U25	74ALS21AD dual 4 input AND	1BB4	1D3,1C6	+5 V Gnd	14 7
U26	74ALS174D hex D FF	1DD4	6D7	+5 V Gnd	16 8
U27	74F244DW TI octal bus DVR	1CC4	2E6	+5 V Gnd	20 10
U28	N82C54–2 Intel prog timer	1BB4	1C6	+5 V Gnd	28 14
U29	74ALS874BDW octal D FF	1DD3	2E3	+5 V Gnd	24 12
U30	74ALS245ADW TI octal bus XFR	1DD3	6C5	+5 V Gnd	20 10

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U31	LM317LZ Motorola 3-terminal regulator	1CC3	7F6	+12 V	3
U32	LM317LZ, Motorola 3-terminal regulator	1BB3	7D6	+12 V	3
U33	DAC-312HS, Analog Devices 12-bit DAC	1DD3	7F4	+12 V –12 V	20 17
U34	DAC-312HS, Analog Devices 12-bit DAC	1CC3	7D4	+12 V –12 V	20 17
U35	DAC-08-CS, Analog Devices 8-bit DAC	1BB3	7C4	+12 V –12 V	1 7
U36	LM317LZ, Motorola 3-terminal regulator	1DD2	2E2	+12 V	3
U37	DAC-312HS, Analog Devices 12-bit DAC	1DD2	2E1	+12 V –12 V	20 17
U38	LM6361N, National operational amp	1CC2	7F4	+12 V –12 V	7 4
U39	LM6361N, National operational amp	1BB2	7D4	+12 V –12 V	7 4
U40	LM675T National PWR operational amp (needs insulator)	1DD1	2C1	+12 V –12 V	5 3
U41	LM6361N, National operational amp	1CC2	7F3	+12 V –12 V	7 4
U42	LM6321N, National buffer	1CC1	7F2	+12 V –12 V	6 1,4,5,8
U43	LM6361N, National operational amp	1BB2	7D3	+12 V –12 V	7 4
U44	LM6321N, National buffer	1BB1	7D2	+12 V –12 V	6 1,4,5,8
U45	74F08D, TI quad 2 input AND	1BB9	3D8	+5 V Gnd	14 7
U46	74F14D, hex schmitt inverter	1BB8	2F7,2E7	+5 V Gnd	14 7
U47	74ALS244BDW TI octal bus DVR	1BB9	3B4	+5 V Gnd	20 10
U48	74ALS244BDW TI octal bus DVR	1BB9	3C4	+5 V Gnd	20 10
U49	74ALS573CDW TI octal latch	1AA9	1E3	+5 V Gnd	20 10
U50	74F521SC octal comparator	1AA9	1F2	+5 V Gnd	20 10

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U51	74F74D dual D FF	1AA9	1C2,7C7	+5 V Gnd	14 7
U52	74ALS175D, TI quad D FF, Q&Q	1AA9	2B5	+5 V Gnd	16 8
U53	74ALS175D, TI quad D FF, Q&Q	1AA8	2F6	+5 V Gnd	16 8
U54	74ALS867ADW sync 8-bit Ctr	1BB7	2D4	+5 V Gnd	24 12
U55	74F139D, dual 2 to 4 decoder	1BB7	3A3,3B3	+5 V Gnd	16 8
U56	74ALS11AD triple 3 input AND	1BB7	2E5,spare spare	+5 V Gnd	14 7
U57	74ALS175D, TI quad D FF, Q&Q	1BB7	2E7	+5 V Gnd	16 8
U58	74ALS08D quad 2 input AND	1BB7	2C5,2F6 2E6,2A5	+5 V Gnd	14 7
U59	74ALS00SC quad 2 input AND	1AA7	2F6,2E6,2C6, 2A6	+5 V Gnd	14 7
U60	74ALS08D quad 2 input AND	1AA7	1C3,1C2,2A2 spare	+5 V Gnd	14 7
U61	74ALS112AD dual J/K FF	1AA7	1C5,1C4	+5 V Gnd	16 8
U62	74F86D quad 2 input EX–OR	1AA7	1D6,1D6 spare,spare	+5 V Gnd	14 7
U63	74ALS08D quad 2 input AND	1BB7	3F8,3E8,3E8 3E8	+5 V Gnd	14 7
U64	74ALS04BD hex inverter	1BB6	6E8,6E7,6E6 6E7,6E7,sp	+5 V Gnd	14 7
U65	74F32D quad 2 input OR	1BB7	1E1,1E1,1E2 6E6	+5 V Gnd	14 7
U66	74F32D quad 2 input OR	1BB6	1D2,1D1,1D1 6E6	+5 V Gnd	14 7
U67	74F138D 1 of 8 decoder	1AA7	2C8	+5 V Gnd	16 8
U68	74F08D quad 2 input AND	1AA6	1C7,1C6,1F6 1E1	+5 V Gnd	14 7
U69	74F138D 1 of 8 decoder	1AA7	2D8	+5 V Gnd	16 8
U70	74F138D 1 of 8 decoder	1AA6	2B8	+5 V Gnd	16 8

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U71	74ALS08D Quad 2 input AND	1BB5	6E7,6E8,6D7 6D6	+5 V Gnd	14 7
U72	74F04D hex inverter	1BB5	1E2,6A2,6D2 7C8,1F4,sp	+5 V Gnd	14 7
U73	74F08D quad 2 input AND	1BB5	6A8,6F4,6F2 6D2	+5 V Gnd	14 7
U74	74ALS174SC hex D FF	1AA5	1A7	+5 V Gnd	16 8
U75	74ALS32D quad 2 input OR	1AA5	2C3,2C3 2B2,2B2	+5 V Gnd	14 7
U76	96S02PC Natl dual one shot	1AA5	7B7, spare	+5 V Gnd	16 7
U77	74F08D quad 2 input AND	1AA5	1E1,3C8 6F6,6D8	+5 V Gnd	14 7
U78	74F138D 1 of 8 decoder	1AA5	2A7	+5 V Gnd	16 8
U79	84F521SC octal comparator	1BB4	1F7	+5 V Gnd	20 10
U80	74F157AD quad 2:1 MUX	1BB4	2D5	+5 V Gnd	16 8
U81	74F138D 1 of 8 decoder	1BB4	1D5	+5 V Gnd	16 8
U82	DS1005S–175, Dallas delay line with 35-ns taps, 175-ns total	1AA4	6F6	+5 V Gnd	14 7
U83	74F32D quad 2 input OR	1AA4	1E5,1E6 1D6,7A5	+5 V Gnd	14 7
U84	74ALS244BDW TI octal bus DVR	1AA4	1E8	+5 V Gnd	20 10
U85	74F32D quad 2 input OR	1BB3	6D3,6D3 6A3,6B3	+5 V Gnd	14 7
U86	74ALS04BD hex inverter	1BB3	6D4,6D3,6C3 6A4,6A3,6A3	+5 V Gnd	14 7
U87	DS1000S–50, Dallas delay line with 10-ns taps, 50-ns total	1AA3	6C3	+5 V Gnd	14 7
U88	LM317LZ, Motorola 3-terminal regulator	1BB3	7C6	+12 V Gnd	3 1
U89	74F244DW TI octal bus Dvr	1AA3	6F4	+5 V Gnd	20 10
U90	DS1000S–50, Dallas delay line with 10-ns taps, 50-ns total	1AA3	6A3	+5 V Gnd	14 7

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U91	74F157AD quad 2:1 MUX	1BB3	7B5	+5 V Gnd	16 8
U92	74F157AD quad 2:1 MUX	1BB2	7B5	+5 V Gnd	16 8
U93	74ALS244BDW TI octal bus Dvr	1AA2	1E8	+5 V Gnd	20 10
U94	96S02PC Natl dual one shot	1AA2	7A7,7A7	+5 V Gnd	16 8
U95	74ALS244BDW TI octal bus Dvr	1AA2	1D8	+5 V Gnd	20 10
U96	LM6361N, National operational amp	1BB1	7C3	+12 V –12 V	7 4
U97	LM6321N, National buffer	1BB1	7C2	+12 V –12 V	6 1,4,5,8
U98	74F244DW TI octal bus Dvr	1AA1	7A5	+5 V Gnd	20 10
U99	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10DD1	5B7	+5 V Gnd	17,22,6 8 14,18,3 5,52
U100	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10DD2	5B6		
U101	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10DD3	5E7		
U102	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10DD4	5E6		
U103	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10CC1	5B4	+5 V Gnd	17,22,6 8,14,18 35,52
U104	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10CC2	5B3		
U105	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10CC3	5E4		
U106	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns	10CC4	5E3		
U107	74F574DW octal D FF	10CC4	6F5	+5 V Gnd	20 10
U108	74ALS574BDW octal D FF	10CC4	3C7	+5 V Gnd	20 10
U109	74ALS244BDW TI octal bus DVR	10BB4	3E4	+5 V Gnd	20 10

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U110	74F574DW octal D FF	10CC5	6E5	+5 V Gnd	20 10
U111	74ALS244BDW TI octal bus DVR	10CC5	3C7	+5 V Gnd	20 10
U112	74F157AD quad 2:1 MUX	10BB5	6A6	+5 V Gnd	16 8
U113	74ALS245ADW TI octal bus XFR	10CC5	6D1	+5 V Gnd	20 10
U114	74F574DW octal D FF	10CC5	6D5	+5 V Gnd	20 10
U115	74ALS867ADW 8-bit sync CTR	10BB5	3A5	+5 V Gnd	24 12
U116	74F244DW TI octal bus DVR	10CC6	6E4	+5 V Gnd	20 10
U117	DS1000S–50, Dallas delay line with 10-ns taps, 50-ns total	10CC6	6A5	+5 V Gnd	14 7
U118	74ALS574BDW octal D FF	10BB6	3A5	+5 V Gnd	20 10
U119	74ALS874BDW octal D FF	10CC6	2A4,2B4	+5 V Gnd	24 12
U120	74ALS867ADW 8-bit sync CTR	10BB6	2B5	+5 V Gnd	24 12
U121	74ALS245ADW TI octal bus XFR	10BB1	3E5	+5 V Gnd	20 10
U122	74ALS244BDW TI octal bus DVR	10AA1	3B7	+5 V Gnd	20 10
U123	74ALS244BDW TI octal bus DVR	10BB1	3D4	+5 V Gnd	20 10
U124	74ALS574BDW octal D FF	10AA1	3A7	+5 V Gnd	20 10
U125	74ALS867ADW 8-bit sync CTR	10BB2	2C5	+5 V Gnd	24 12
U126	74ALS574BDW octal D FF	10AA2	3B5	+5 V Gnd	20 10
U127	74ALS874BDW octal D FF	10BB3	2C4,2C4	+5 V Gnd	24 12
U128	74ALS867ADW 8-bit sync CTR	10AA3	3B5	+5 V Gnd	24 12
U129	74ALS244BDW TI octal bus DVR	10BB3	3C4	+5 V Gnd	20 10

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U130	74ALS244BDW TI octal bus DVR	10AA3	3F4	+5 V Gnd	20 10
U131	74ALS08D quad 2 input AND	10BB4	2C3,2C3, 2B3 spare	+5 V Gnd	14 7
U132	74F74D dual D FF	10BB4	2A3,2C2	+5 V Gnd	14 7
U133	74ALS244BDW TI octal bus DVR	10AA4	3E4	+5 V Gnd	20 10
U134	74ALS245ADW TI octal bus XVR	10BB4	3E5	+5 V Gnd	20 10
U135	74F157AD quad 2:1 MUX	10BB5	6B6	+5 V Gnd	16 8
U136	74ALS867ADW 8-bit sync CTR	10BB5	6B7	+5 V Gnd	24 12
U137	74ALS244BDW TI octal bus DVR	10BB6	3A4	+5 V Gnd	20 10
U138	74F09D, quad 2-input AND (O. C.)	10AA6	1E1,2A8 spare,sp	+5 V Gnd	14 7
U139	74ALS04BD hex inverter	10AA6	2F7,2E6, (4–spares)	+5 V Gnd	14 7
U140	74ALS245ADW TI octal bus XFR	10BB6	1A8	+5 V Gnd	20 10
U141	74ALS11AD triple 3-input AND	10AA6	2B1,spare, spare	+5 V Gnd	14 7
U142	74ALS11AD triple 3-input AND	10AA6	2C2,2B2 spare	+5 V Gnd	14 7
U143	74ALS04BD hex inverter	10AA6	2C2,2C1, 2B2,2B1, (2-spare)	+5 V Gnd	14 7
U144	74F08D, quad 2-input AND	10AA6	7B7,7A6, 7A2 (3-spares)	+5 V Gnd	14 7
U145	74F109D, dual J-/K FF	10AA7	7A3,7A2	+5 V Gnd	16 8
U146	74F260D, dual 5-input NOR	10AA7	7B6,spare	+5 V Gnd	14 7
U147	74ALS245ADW TI octal bus XFR	10AA9	1B8	+5 V Gnd	20 10
U148	DS1000S–50, Dallas delay line with 10-ns taps, 50-ns total	10BB5 (chip glued upside down)	2A2	+5 V Gnd	14 7

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
U149	74F32D quad 2-input OR	10BB7 (chip glued upside down)	6F6	+5 V Gnd	14 7
Y1	SG–615P(OE), Epson 20-MHz surface mt crystal oscillator	1BB5	2D6	+5 V Gnd	4 2
R1	420CK103X2PD, 10K SIP, Sprague 10 pins	1DD6	4C2–(8) 6D8	+5 V	1
R2	420CK103X2PD, 10K SIP, Sprague 10 pins	1DD6	4B2–(8) 6C8	+5 V	1
R3	420CK103X2PD, 10K SIP, Sprague 10 pins	1CC6	4D2–(8)	+5 V	1
R4	420CK103X2PD, 10K SIP, Sprague 10 pins	1CC6	4E2–(8)	+5 V	1
R5	420CK103X2PD, 10K SIP, Sprague 10 pins	1BB6	4F3–(5)	+5 V	1
R6	420CK103X2PD, 10K SIP, Sprague 10 pins	1BB6	1B4–(7) 7B7	+5 V	1
R7	420CK103X2PD, 10K SIP, Sprague 10 pins	1DD5	6E4–(4) 6B4(4),7A6	+5 V	1
R8	420CK103X2PD, 10K SIP, Sprague 10 pins	1BB4	1F7–(8),7C7	+5 V	1
R9	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1CC3	7F5		
R10	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1CC3	7F6		
R11	Bourns 3339P–1–102 cermet 4-turn 1K pot	1CC3	7E6		
R12	420CK103X2PD, 10K SIP, Sprague 10 pins	1CC3	1B5–(9)	+5 V	1
R13	9C12063A4750FKH Phillips 475-ohm (1%) 1/8 W chip resistor	1CC3	7E6		
R14	9C12063A2490FKH Phillips 249-ohm (1%) 1/8 W chip resistor	1CC3	7F6		
R15	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC3	7D4		
R16	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1CC3	7D6		
R17	9C12063A4750FKH Phillips 475-ohm (1%) 1/8 W chip resistor	1CC3	7D6		

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
R18	9C12063A2490FKH Phillips 249-ohm (1%) 1/8 W chip resistor	1CC3	7D5	
R19	Bourns 3339P–1–102 cermet 4–turn 1K pot	1BB3	7D6	
R20	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1DD3	7D5	
R21	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC3	7D4	
R22	9C12063A2490FKH Phillips 249-ohm (1%) 1/8 W chip resistor	1CC2	2E2	
R23	9C12063A4750FKH Phillips 475-ohm (1%) 1/8 W chip resistor	1CC3	7B6	
R24	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1BB2	7D3	
R25	9C12063A1003FKH Phillips l00K-ohm (1%) 1/8 W chip resistor	1DD2	2F5	
R26	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1DD2	2E2	
R27	9C12063A2000FKH Phillips 200-ohm (1%) 1/8 W chip resistor	1DD2	2D2	
R28	Bourns 3339P–1–102 cermet 4-turn 1K pot	1DD2	2E2	
R29	9C12063A4750FKH Phillips 475-ohm (1%) 1/8 W chip resistor	1CC2	2E2	
R30	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7F4	
R31	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1CC2	7E3	
R32	Bourns 3339P–1–202 cermet 4-turn 2K pot	1CC2	7E3	
R33	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7F4	
R34	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7F4	
R35	Bourns 3339P–1–202 cermet 4-turn 2K pot	1BB2	7D3	
R36	KOA RM73B2B–J–10K, 10K-ohm (5%), 1206, 1/4 W chip resistor	1DD2	2E4	
R37	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	1DD2	2D2	

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
R38	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1CC2	7E4		
R39	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7F3		
R40	Bourns 3339P–1–502 cermet 4-turn 5K pot	1CC2	7F3		
R41	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1CC2	7E4		
R42	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7F3		
R43	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	1CC2	7D3		
R44	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	1CC2	7E3		
R45	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1CC2	7E4		
R46	Bourns 3339P–1–502 cermet 4-turn 5K pot	1CC2	7E3		
R47	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	1CC1	7E3		
R48	9C12063A2491FKH Phillips 2490-ohm (1%) 1/8 W chip resistor	1DD1	2D1		
R49	KOA RM73B2B–J–10, 10-ohm (5%), 1206, 1/4 W chip resistor	1DD1	2C1		
R50	KOA RM73B2B–J–100. 100-ohm (5%), 1206, 1/4 W chip resistor	1CC1	7F2		
R51	9C12063A2000FKH Phillips 200-ohm (1%) 1/8 W chip resistor	1DD1	2C2		
R52	KOA RM73B2B–J–100. 100-ohm (5%), 1206, 1/4 W chip resistor	1CC1	7F2		
R53	KOA RM73B2B–J–100. 100-ohm (5%), 1206, 1/4 W chip resistor	1CC1	7D2		
R54	KOA RM73B2B–J–100. 100-ohm (5%), 1206, 1/4 W chip resistor	1CC1	7D2		
R55	420CK103X2PD, 10K SIP, Sprague 10 pins	1AA8	1C5,1C4,1C2, 1C6(2),1D7(2) 1D5, spare	+5 V	1
R56	420CK103X2PD, 10K SIP, Sprague 10 pins	1AA8	1F4(6) 3-spare	+5 V	1

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins	
R57	420CK103X2PD, 10K SIP, Sprague 10 pins	1AA7	2B6,2D3,2C3, 2B3,2A8,2B8, 2C8,2D8, spare	+5 V	1
R58	Bourns 3339P–1–204 cermet 4-turn 200K pot	1AA6	7C7		
R59	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1AA6	7B7		
R60	420CK103X2PD, 10K SIP, Sprague 10 pins	1AA5	7A6,2B2(3) 2C2(3),3F8 3F5	+5 V	1
R61	420CK103X2PD, 10K SIP, Sprague 10 pins	1AA5	2F4(4),2F5 2D4,7A7,7A6 7B2	+5 V	1
R62	Bourns 3339P–1–102 cermet 4–turn 1K pot	1BB3	7C6		
R63	9C12063A2490FKH Phillips 249-ohm (1%) 1/8 W chip resistor	1BB3	7C6		
R64	9C12063A3921FKH Phillips 3920-ohm (1%) 1/8 W chip resistor	1BB3	7C5		
R65	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1AA3	7A7		
R66	Bourns 3339P–1–204 cermet 4-turn 200K pot	1AA3	7A7		
R67	Bourns 3339P–1–104 cermet 4-turn 100K pot	1AA3	7A7		
R68	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1AA3	7A6		
R69	9C12063A3921FKH Phillips 3920-ohm (1%) 1/8 W chip resistor	1BB3	7C5		
R70	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1BB2	7D4		
R71	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1BB2	7D4		
R72	Bourns 3339P–1–202 cermet 4-turn 2K pot	1BB2	7A3		
R73	9C12063A1001 FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1BB2	7C3		
R74	9C12063A6340 FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1BB2	7B4		
R75	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1BB2	7D3		

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
R76	Bourns 3339P–1–202 cermet 4-turn 2K pot	1BB2	7C3	
R77	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1BB2	7C3	
R78	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	1BB2	7E3	
R79	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	1BB2	7B3	
R80	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	1BB1	7D3	
R81	9C12063A1000FKH Phillips 100-ohm (1%) 1/8 W chip resistor	1BB1	7C3	
R82	9C12063A9090FKH Phillips 909-ohm (1%) 1/8 W chip resistor	1BB2	7C3	
R83	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	1BB1	7C3	
R84	9C12063A47R5FKH Phillips 47.5-ohm (1%) 1/8 W chip resistor	1AA1	7C2	

Ref#	Item and Manufacturer	Board Location		Schematic
C1 thru C7	12065C104KATAMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C1 – 1CC5 C2 – 1CC5 C3 – 1BB4 C4 – 1CC4	C5 – 1DD4 C6 – 1CC3 C7 – 1CC3	3B2,3A1
C8 thru C9	12061C103KAT050M AVX/KYOCERA 0.01 Mfd 1206 XTR 100-V 10% chip capacitor (unmarked)	C8 – 1DD3 C9 – 1DD3		7E5,7D5
C10 thru C20	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C10 – 1CC3 C11 – 1CC3 C12 – 1CC3 C13 – 1CC3 C14 – 1CC3 C15 – 1BB3	C16 – 1CC3 C17 – 1CC2 C18 – 1CC2 C19 – 1CC2 C20 – 1BB2	2E2,7F2,7F6, 2E3,7D5,7B3, 7F5,7E3,7E3, 2E2,7D3
C21	NMC 1206 ceramic 220 Pf NPO chip cap (unmarked)	C21 – 1BB2		7A8
C22 thru C23	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 XTR 50-V 10% chip capacitor (unmarked)	C22 – 1CC2 C23 – 1CC2		7D6 7F5
C24	12061C103KAT050M AVX/KYOCERA 0.01 Mfd 1206 X7R 100-V 10% chip capacitor (unmarked)	C24 – 1CC2		2E2
C25 thru C33	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C25 – 1CC2 C26 – 1CC2 C27 – 1CC2 C28 – 1CC2 C29 – 1CC2	C30 – 1CC2 C31 – 1BB2 C32 – 1CC1 C33 – 1CC1	7F4,2D1,7D4, 7E3,7C5,7D3, 7B4,7F3,2C1
C34	Mouser #555–10C25, 10 Mfd, 25-V, ELNA tant surface mt cap.	C34 – 1AA2		3C1
C35 thru C42	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C35 – 1BB1 C36 – 1BB1 C37 – 1BB1 C38 – 1BB1	C39 – 1CC1 C40 – 1DD1 C41 – 1DD1 C42 – 1DD1	7D3;7B2,7D2, 7D2,7E2,7E4, 7C4,7D5
C43	Mouser #555–10C25 10 Mfd, 25-V, ELNA tant surface mt cap.	C43 – 1AA1		3A1
C44 thru C55	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C44 – 1BB9 C45 – 1AA9 C46 – 1AA9 C47 – 1AA9 C48 – 1AA9 C49 – 1AA9	C50 – 1BB8 C51 – 1BB8 C52 – 1AA8 C53 – 1AA8 C54 – 1BB8 C55 – 1BB7	3C2,3C2,3B2, 3B2,3B1,3C2, 3B2,3B1,3B2, 3C2,3B2,3B2

Ref#	Item and Manufacturer	Board Location		Schematic
C56 thru C60	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C56 – 1BB7 C57 – 1AA7 C58 – 1BB7	C59 – 1BB6 C60 – 1AA6	3A2,3B2,3A1, 3A1,3A2
C61	NMC 1206 Ceramic 100 Pf J NPO chip cap (unmarked)	C61 – 1AA6		7B8
C62 thru C68	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C62 – 1AA6 C63 – 1AA6 C64 – 1BB5 C65 – 1AA4	C66 – 1BB4 C67 – 1AA3 C68 – 1AA3	3A1,3A1,3B1, 3B1,3A1,3A2, 3A2
C69	12061C103KAT050M AVX/KYOCERA 0.01 Mfd 1206 X7R 100-V 10% chip capacitor (unmarked)	C69 – 1BB3		7B5
C70 thru C74	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 XTR 50-V 10% chip capacitor (unmarked)	C70 – 1BB2 C71 – 1BB2 C72 – 1BB2	C73 – 1AA2 C74 – 1AA2	7C6,7C3,7D4, 3B1,3B1
C75	NMC 1206 ceramic 10 Pf J NPO chip cap (unmarked)	C75 – 1AA2		7A7
C76 thru C79	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 XTR 50-V 10% chip capacitor (unmarked)	C76 – 1AA2 C77 – 1BB2	C78 – 1BB2 C79 – 1BB2	3A2,7B3,3B1, 7C2
C80	Mouser #555–10C25 10 Mfd, 25-V, ELNA tant surface mt cap.	C80 – 1AA2		3C1
C81 thru C82	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C81 – 1BB1 C82 – 1AA1		7C3,3B1
C83 thru C94	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C83 – 10CC1 C84 – 10CC1 C85 – 10CC4 C86 – 10CC4 C87 – 10DD4 C88 – 10CC5	C89 – 10CC5 C90 – 10DD5 C91 – 10CC5 C92 – 10DD5 C93 – 10DD6 C94 – 10DD5	3B1,3B1,3B1, 3B1,3A2,3B1, 3B1,3A1,3B1, 3A1,3A1,3B1
C95 thru C106	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C95 – 10AA1 C96 – 10AA1 C97 – 10BB1 C98 – 10AA1 C99 – 10AA1 C100 –10BB1	C101 – 10BB2 C102 – 10BB2 C103 – 10AA2 C104 – 10AA2 C105 – 10AA2 C106 – 10BB2	3B2,3B2,3B2, 3B2,3B2,3B2, 3B1,3B1,3C1, 3C1,3C1,3B1

Ref#	Item and Manufacturer	Board Location		Schematic
C107 thru C118	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C107 – 10BB3 C108 – 10AA3 C109 – 10BB3 C110 – 10AA3 C111 – 10BB3 C112 – 10BB3	C113 – 10BB3 C114 – 10AA3 C115 – 10BB3 C116 – 10BB3 C117 – 10BB4 C118 – 10BB6	3B1,3B1,3B2, 3C1,3C1,3B2, 3C1,3B1,3B2, 3B1,3B1,3B1
C119 thru C123	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C119 – 10BB6 C120 – 10BB6 C121 – 10AA7	C122 – 10BB7 C123 – 10AA8	3B1,3B1,3B1, 3B1,3B1

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
TP1	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1DD6	4C1	DGND 1
TP2	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1DD6	4B1	DGND 1
TP3	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1CC6	4D1	DGND 1
TP4	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1CC6	4D1	DGND 1
TP5	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1CC4	1D4	DGND 1
TP6	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1CC4	1B4	DGND 1
TP7	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1CC3	1A5	DGND 1
TP8	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1BB8	3B4	DGND 1
TP9	TSW–110–14–H–S, SAMTEC 10-pin,. 0.25-in.-sq. post header	1BB6	3A4	DGND 1
TP10	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1BB6	1A5	DGND 1
TP11	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA6	2B7	DGND 1
TP12	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA6	2C7	DGND 1
TP13	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA6	2D7	DGND 1
TP14	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA6	1C8,1D7,1D3 1E1,1F2,1D1	DGND 1
TP15	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA5	2A7	DGND 1
TP16	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA5	2C1,2B1,3E7 7A1	DGND 1
TP17	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA5	1F5	DGND 1
TP18	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA5	1E3	DGND 1
TP19	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA5	1E5	DGND 1
TP20	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1AA2	7A4	DGND 1

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
P1	"AT" board 62 pins	—	layer 1 Assembly Dwg	
P2	"AT" board 36 pins	—	layer 1 Assembly Dwg	
P3	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6D3	DGND 3
P4	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6D4	DGND 3
P5	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6D4	DGND 3
P6	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6D4	DGND 3
P7	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6A5	
P8	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	7A8	DGND 1
P9	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6B3	DGND 3
P10	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD4	6B4	DGND 3
P11	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD3	2E4	DGND 2
P12	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC3	2F5	DGND 2
P13	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA7	2B3	
P14	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD1	2C1	

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
P15	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD1	2C1	AGND 2
P16	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD1	2E4	
P17	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC1	2F4	
P18	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC6	6B4	DGND 3
P19	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC6	3F5	DGND 3
P20	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1BB6	2E5	
P21	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1BB8	2D4	
P22	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA8	1C7	
P23	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA8	1C2	
P24	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA7	2C3	
P25	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA7	2D3	
P26	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA7	2C3	
P27	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA6	3E8	DGND 1
P28	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1BB6	2B2	

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
P29	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA5	7B6	DGND 1
P30	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA5	7A6	DGND 1
P31	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA5	1C3	
P32	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1BB5	6B4	DGND 3
P33	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA4	6F6	
P34	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA5	2B2	DGND 6
P34	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA5	2B2	
P35	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA3	1C1	
P36	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA2	2A1	
P37	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD3	2F5	
E1	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD2	2F8	DGND 2
E2	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1DD2	2E8	DGND 2
E3	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC1	7E2	
E4	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC1	7D2	AGND 2

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
E5	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC1	7F2	
E6	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1CC1	7F2	AGND 2
E7 thru E10	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing (quantity 2)	1AA8	2D4	
E11 thru E13	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA8	2D4	
E14	TSW–101–14–H–S, SAMTEC 1 pin, 0.25-in.-sq. post (not used)	1BB5	3A5	
E15	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing	1AA1	7C1	AGND 2
SW1	Grayhill 76SB08, 8-position DIP Sw	1BB8	1F8	
SW2	Grayhill 76SB02, 2-position DIP Sw	1AA8	1D7	
SW3	Grayhill 76SB08, 8-position DIP Sw	1AA8	1F4	
VR1 thru VR6	1N752A 5. 6-V zener diode	VR1 – 1CC2 VR2 – 1CC2 VR3 – 1CC2 VR4 – 1BB2 VR5 – 1BB2 VR6 – 1BB2		7E3,7E3,7D3, 7D3,7B3,7B3
J3	Pomona Model 5365 SMB male right-angle bulkhead connector	1CC1	7F1	
J4	Pomona Model 5365 SMB male right-angle bulkhead connector	1CC1	7D1	
J5	SAMTEC 6-pin, 0.25-in.-sq. post in double row right-angle shroud strip on 0.100 centers BST–103–09–S–D–318–RA	1CC1	2F8,2E8 2F4,2E4	
J6	SAMTEC 36-pin, 0.25-in.-sq. post in double row right-angle shroud strip on 0.100 centers, BST–118–09–G– D–318–RA	1BB1	6F3,6E3 6C3,7A4 7A1	DGND 2
J7	Pomona Model 5365 SMB male right-angle bulkhead connector	1AA1	7C1	

Ref#	Item and Manufacturer	Board Location	Schematic Locations	Power and Ground Pins
J8	TSW–110–14–H–S SAMTEC 10-pin, 0.25-in.-sq. post header (5 pins used)	1DD2	2D4,2F8 2E8,2F4	DGND 2
J9	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing.	1DD1	2C1	AGND 1
J10	TSW–110–14–H–S, SAMTEC, 10-pin, 0.25-in.-sq. post with 0.100-in. spacing.	1CC4	6E3	DGND 1
J11	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1BB3	6C4	DGND 1
J12	TSW–110–14–H–S, SAMTEC 10-pin, 0.25-in.-sq. post header	1BB3	6F3	DGND 1

MISCELLANEOUS

1	Rear Bracket. Globe Mfg, #G01 (Basic Blank) Bracket. (modified at NRaD)	
1	Nylon 6–32, 3/4-in. machine screw for U40.	1DD1
1	Nylon 6–32 nut for machine screw at U40.	1DD1
1	Insulator for U40 Wakefield #175–6–240P. Kapton insulator for type 270 AB heat sink	1DD1
1	Set of films for all 10 layers.	
1	Fabricate 10 layered printed wiring board (PWB) & conduct electrical conformity checks. Crown Circuits.	
1	Solder 448 components to layers 1 & 10 of the printed wiring board. North Star–Electronics.	
448	Total components for Volumetric #2 board.	

16. VOLUMETRIC BOARD #2 PARTS INVENTORY INFORMATION

The Volumetric Board #2 Parts Inventory lists the volumetric #2 components by part types, quantity of that item on the board, designation (U Numbers, R Numbers, etc.) and the board location of these parts.

Note: Board location Layer 10 (Backside) is labeled 10xxy.

This list is normally used to order the parts for the boards or to kit the parts needed to assemble the board.

QTY	Item and Manufacturer	Designation	Board Location
1	74ALS00SC [14-pin SOIC] quad 2 input NAND	U59	1AA7
4	74ALS04BD [14-pin SOIC] hex inverter	U64,U86,U139, U143	1BB6,1BB3,10AA6, 10AA6
5	74ALS08D [14-pin SOIC] quad 2 input AND	U58,U60,U63, U71,U131	1BB7,1AA7,1BB7, 1BB5,10BB4
3	74ALS11AD [14-pin SOIC] triple 3 input AND	U56,U141, U142	1BB7,10AA6, 10AA6
1	74ALS21AD [14-pin SOIC] dual 4 input AND	U25	1BB4
1	74ALS32D [14-pin SOIC] quad 2 input OR	U75	1AA5
1	74ALS112AD [16-pin SOIC] dual J–K FF	U61	1AA7
3	74ALS174D [16-pin SOIC] TI hex D FF	U17,U26,U74	1DD5,1DD4,1AA5
3	74ALS175D, TI [16-pin SOIC] quad D FF, Q&/Q	U52,U53,U57	1AA9,1AA8,1BB7
15	74ALS244BDW [20-pin SOIC] TI octal bus DVR	U16,U20,U47, U48,U84,U93, U95,U109,U111, U122,U123,U129, U130,U133,U137	1BB5,1BB5,1BB9, 1BB9,1AA4,1AA2, 1AA2,10BB4,10CC5, 10AA1,10BB1,10BB3, 10AA3,10AA4,10BB6
9	74ALS245ADW [20-pin SOIC] TI octal bus XFR	U13,U18,U19, U30,U113,U121, U134,U140,U147	1DD5,1CC5,1CC5, 1DD3,10CC5,10BB1, 10BB4,10BB6,10AA9
1	74ALS573CDW [20-pin SOIC] TI octal Latch	U49	1AA9
4	74ALS574BDW [20-pin SOIC] octal D FF	U108,U118, U124,U126	10CC4,10BB6, 10AA1,10AA2

QTY	Item and Manufacturer	Designation	Board Location
6	74ALS867ADW [24-pin SOIC] sync 8-bit CTR	U54,U115,U120, U125,U128,U136	1BB7,10BB5,10BB6, 10BB2,10AA3,10BB5
4	74ALS874BDW [24-pin SOIC] octal D FF	U23,U29,U119, U127	1CC4,1DD3,10CC6, 10BB3
1	N82C54–2 [28-pin PLCC] 10-MHz Intel prog timer	U28	1BB4
4	LM317LZ, National 3-terminal regulator	U31,U32,U36, U88	1CC3,1BB3,1DD2, 1BB3
1	DAC–08–CS, Analog Devices 8-bit DAC	U35	1BB3
3	DAC–312HS, Analog Devices 12-bit DAC [20-pin SOIC]	U33,U34,U37	1DD3,1CC3,1DD2
3	LM6321N, National buffer [8-pin DIP]	U42,U44,U97	1CC1,1BB1(2)
5	LM6361N, National operational amp [8-pin DIP]	U38,U39,U41, U43,U96	1CC2,1BB2,1CC2, 1BB2,1BB1
1	74F04D [14-pin SOIC] hex inverter	U72	1BB5
5	74F08D, TI [14-pin SOIC] quad 2 input AND	U45,U68,U73, U77,U144	1BB9,1AA6,1BB5, 1AA5,10AA6
1	74F09D, quad 2 [14-pin SOIC] input AND (O.C.)	U138	10AA6
1	74F14D, Hex [14-pin SOIC] Schmitt inverter	U46	1BB8
5	74F32D [14-pin SOIC] quad 2 input OR	U65,U66,U83, U85,U149	1BB7,1BB6,1AA4, 1BB3,10BB7
2	74F74D [14-pin SOIC] dual D FF	U51,U132	1AA9,10BB4
1	74F86D [14-pin SOIC] quad 2 input EX–OR	U62	1AA7
1	74F109D, dual J–/K FF [16-pin SOIC]	U145	10AA7
6	74F138D [16-pin SOIC] 3 to 8 decoder	U24,U67,U69, U70,U78,U81	1BB4,1AA7,1AA7, 1AA6,1AA5,1BB4
1	74F139D dual 2 to 4 decoder	U55	1BB7

QTY	Item and Manufacturer	Designation	Board Location
6	74F157AD [16-pin SOIC] 2:1 MUX	U21,U80,U91, U92,U112,U135	1DD5,1BB4,1BB3, 1BB2,10BB5,10BB5
5	74F244DW [20-pin SOIC] TI octal bus DVR	U14,U27,U89, U98,U116	1CC5,1CC4,1AA3, 1AA1,10CC6
1	74F260D, dual 5-input NOR [14-pin SOIC]	U146	10AA7
2	74F521SC [20-pin SOIC] octal comparator	U50,U79	1AA9,1BB4
4	74F574DW [20-pin SOIC] octal D FF	U22,U107,U110, U114	1CC4,10CC4,10CC5, 10CC5
16	IDT 7006S35J, 16K x 8 dual-port RAM, 35 ns [68-pin PLCC]	U1,U2,U3,U4, U5,U6,U7,U8, U99,U100,U101, U102,U103,U104, U105,U106	1DD9,1DD8,1DD8,1DD7, 1CC9,1CC8,1CC8,1CC7, 10DD1,10DD2,10DD3, 10DD4,10CC1,10CC2, 10CC3,10CC4
4	SEEQ LQ28HC32–55 4K x 8, 55-ns EEPROM [32-pin LCC]	U9,U10,U11,U12	1DD5,1CC5,1CC5,1BB5
1	IDT 6116SA25Y [24-pin SOJ] 2K x 8, 25-ns RAM	U15	1CC5
2	96S02PC Natl dual one shot [16-pin DIP]	U76,U94	1AA5,1AA2
4	DS1000S–50, Dallas delay line with 10-ns taps, 50-ns total [14-pin SOIC]	U87,U90,U117 U148	1AA3,1AA3,10CC6, 10BB5
1	DS1005S–175, Dallas delay line with 35-ns taps, 175-ns total [14-pin SOIC]	U82	1AA4
1	LM675T, National Pwr operational amp (needs insulator) [5-pin]	U40	1DD1
1	SG–615P(OE), Epson 20-MHz surface mt crystal oscillator [4-pin SOIC special]	Y1	1BB5
14	420CK103X2PD, 10K SIP, Sprague [10-pin SIP]	R1,R2,R3,R4, R5,R6,R7,R8, R12,R55,R56,R57, R60,R61	1DD6,1DD6,1CC6,1CC6, 1BB6,1BB6,1DD5,1BB4, 1CC3,1AA8,1AA8,1AA7, 1AA5,1AA5

QTY	Item and Manufacturer	Designation	Board Location
1	9C12063A47R5FKH Phillips 47.5-ohm (1%) 1/8 W chip resistor	R84	1AA1
1	9C12063A1000FKH Phillips 100-ohm (1%) 1/8 W chip resistor	R81	1BB1
2	9C12063A2000FKH Phillips 200-ohm (1%) 1/8 W chip resistor	R27,R51	1DD2,1DD1
4	9C12063A2490FKH Phillips 249-ohm (1%) 1/8 W chip resistor	R14,R18,R22, R63	1CC3,1CC3,1CC2, 1BB3
4	9C12063A4750FKH Phillips 475-ohm (1%) 1/8 W chip resistor	R13,R17,R23, R29	1CC3,1CC3,1CC3, 1CC2
8	9C12063A6340FKH Phillips 634-ohm (1%) 1/8 W chip resistor	R24,R31,R38, R41,R70,R71, R74,R79	1BB2,1CC2,1CC2, 1CC2,1BB2,1BB2, 1BB2,1BB2
1	9C12063A9090FKH Phillips 909-ohm (1%) 1/8 W chip resistor	R82	1BB2
15	9C12063A1001FKH Phillips 1K-ohm (1%) 1/8 W chip resistor	R15,R21,R30, R33,R34,R39, R42,R45,R59, R65,R68,R73, R75,R77,R78	1CC3,1CC3,1CC2, 1CC2,1CC2,1CC2, 1CC2,1CC2,1AA6 1AA3,1AA3,1BB2, 1BB2,1BB2,1BB2
5	9C12063A2001FKH Phillips 2K-ohm (1%) 1/8 W chip resistor	R43,R44,R47, R80,R83	1CC2,1CC2,1CC1, 1BB1,1BB1
1	9C12063A2491FKH Phillips 2490-ohm (1%) 1/8 W chip resistor	R48	1DD1
2	9C12063A3921FKH Phillips 3920-ohm (1%) 1/8 W chip resistor	R64,R69	1BB3,1BB3
6	9C12063A8251FKH Phillips 8250-ohm (1%) 1/8 W chip resistor	R9,R10,R16,R20, R26,R37	1CC3,1CC3,1CC3,1DD3, 1DD2,1DD2
1	9C12063A1003FKH Phillips 100K-ohm (1%) 1/8 W chip resistor	R25	1DD2

QTY	Item and Manufacturer	Designation	Board Location
1	KOA RM73B2B–J–10. 10-ohm (5%), 1206, 1/4 W chip resistor	R49	1DD1
4	KOA RM73B2B–J–100. 100-ohm (5%), 1206, 1/4 W chip resistor	R50,R52,R53,R54	1CC1,1CC1,1CC1,1CC1
1	KOA RM73B2B–J–10K 10K-ohm (5%),1206 1/4 W chip resistor	R36	1DD2
4	Bourns 3339P–1–102 Cermet 4-turn 1K pot [3-pin thru hole]	R11,R19,R28 R62	1CC3,1BB3,1DD2, 1BB3
4	Bourns 3339P–1–202 Cermet 4-turn 2K pot	R32,R35,R72,R76	1CC2,1BB2(3)
2	Bourns 3339P–1–502 Cermet 4-turn 5K pot	R40,R46	1CC2(2)
1	Bourns 3339P–1–104 Cermet 4-turn 100K pot	R67	1AA3
2	Bourns 3339P–1–204 Cermet 4-turn 200K pot	R58,R66	1AA6,1AA3
113	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked)	C1,C2,C3, C4,C5,C6, C7,C10,C11, C12,C13,C14, C15,C16,C17,	1CC5,1CC5,1BB4, 1CC4,1DD4,1CC3, 1CC3,1CC3,1CC3, 1CC3,1CC3,1CC3, 1BB3,1CC3,1CC2,
		C18,C19,C20, C22,C23,C25, C26,C27,C28, C29,C30,C31, C32,C33,C35,	1CC2,1CC2,1BB2, 1CC2,1CC2,1CC2, 1CC2,1CC2,1CC2, 1CC2,1CC2,1BB2, 1CC1,1CC1,1BB1,
		C36,C37,C38, C39,C40,C41, C42,C44,C45, C46,C47,C48, C49,C50,C51,	1BB1,1BB1,1BB1, 1CC1,1DD1,1DD1, 1DD1,1BB9,1AA9, 1AA9,1AA9,1AA9, 1AA9,1BB8,1BB8,
		C52,C53,C54, C55,C56,C57, C58,C59,C60, C62,C63,C64, C65,C66,C67,	1AA8,1AA8,1BB8, 1BB7,1BB7,1AA7, 1BB7,1BB6,1AA6, 1AA6,1AA6,1BB5, 1AA4,1BB4,1AA3,

QTY	Item and Manufacturer	Designation	Board Location
	12065C104KATMA AVX/KYOCERA 0.1 Mfd 1206 X7R 50-V 10% chip capacitor (unmarked) (continued)	C68,C70,C71, C72,C73,C74, C76,C77,C78, C79,C81,C82, C83,C84,C85,	1AA3,1BB2,1BB2, 1BB2,1AA2,1AA2, 1AA2,1BB2,1BB2, 1BB2,1BB1,1AA1, 10CC1,10CC1,10CC4,
		C86,C87,C88, C89,C90,C91, C92,C93,C94, C95,C96,C97, C98,C99,C100,	10CC4,10DD4,10CC5, 10CC5,10DD5,10CC5, 10DD5,10DD6,10DD5, 10AA1,10AA1,10BB1, 10AA1,10AA1,10BB1,
		C101,C102,C103, C104,C105,C106, C107,C108,C109, C110,C111,C112, C113,C114,C115,	10BB2,10BB2,10AA2, 10AA2,10AA2,10BB2, 10BB3,10AA3,10BB3, 10AA3,10BB3,10BB3, 10BB3,10AA3,10BB3,
		C116,C117,C118, C119,C120,C121, C122,C123	10BB3,10BB4,10BB6, 10BB6,10BB6,10AA7, 10BB7,10AA8
4	12061C103KAT050M AVX/KYOCERA 0.01 Mfd 1206 X7R 100-V 10% chip capacitor (unmarked) (red dot)	C8,C9,C24,C69	1DD3,1DD3,1CC2,1BB3
1	NMC 1206 ceramic 10 Pf J NPO chip cap (unmarked) (black dot)	C75	1AA2
1	NMC 1206 ceramic 100 Pf J NPO chip cap (unmarked) (red & black dots)	C61	1AA6
1	NMC 1206 ceramic 220 Pf J NPO chip cap (unmarked) (all black between ends)	C21	1BB2
3	Mouser #555–10C25 10 Mf, 25-V, ELNA Tant Surface Mt Cap.	C34,C43,C80	1AA2,1AA1,1AA2
24	TSW–110–14–H–S SAMTEC 10-pin, 0.25-in.-sq. post header	TP1,TP2,TP3, TP4,TP5,TP6, TP7,TP8,TP9, TP10,TP11,TP12, TP13,TP14,TP15,	1DD6,1DD6,1CC6, 1CC6,1CC4,1CC4, 1CC3,1BB8,1BB6, 1BB6,1AA6,1AA6, 1AA6,1AA6,1AA5,

QTY	Item and Manufacturer	Designation	Board Location
24	TSW–110–14–H–S SAMTEC 10-pin, 0.25-in.-sq.	TP16,TP17,TP18, TP19,TP20	1AA5,1AA5,1AA5, 1AA5,1AA2
	post header (continued)	J8,J10,J11, J12	1DD2,1CC4,1BB3, 1BB3
20	TSW–103–14–H–S, SAMTEC 3-pin, 0.25-in.-sq. post with 0.100-in. spacing. *combine 2- & 3-pin headers	P3,P4,P5,P6, P7,P8,P9,P10, P18,P19,P24, P26(2),P28,P29, P30,P32,P34*,P36	1DD4,1DD4,1DD4,1DD4, 1DD4,1DD4,1DD4,1DD4, 1CC6,1CC6,1AA7, 1AA7(2),1BB6,1AA5, 1AA5,1BB5,1AA5,1AA2
		(E11–E13)	1AA8
34	TSW–102–14–H–S, SAMTEC 2-pin, 0.25-in.-sq. post with 0.100-in. spacing.	P11,P12,P13(2), P14,P15,P16,P17, P20,P21(2),P22, P23(2),P25(2), P27,P31,P33(2),	1DD3,1CC3,1AA7, 1DD1,1DD1,1DD1,1CC1, 1BB6,1BB8,1AA8, 1AA8,1AA7, 1AA6,1AA5,1AA4
	*combine 2- & 3-pin headers	P34(2)*,P35,P37	1AA5,1AA3,1DD3
		E1,E2,E3,E4, E5,E6, (E7–E8), (E9–E10), E15	1DD2,1DD2,1CC1,1CC1, 1CC1,1CC1, 1AA8, 1AA8, 1AA1
		J9	1DD1
2	Grayhill 76SB08 8-position DIP sw	SW1,SW3	1BB8,1AA8
1	Grayhill 76SB02 2-position DIP sw	SW2	1AA8
6	1N752A 5.6-V zener diode	VR1,VR2,VR3, VR4,VR5,VR6	1CC2,1CC2,1CC2, 1BB2,1BB2,1BB2,
3	Pomona Model 5365 SMB male right-angle bulkhead connector	J3,J4,J7	1CC1,1CC1,1AA1
1	SAMTEC 6-pin, 0.25-in.-sq. post in double row right-angle shroud strip on 0.100 centers. BST–103–09–S–D–318–RA	J5	1CC1
1	SAMTEC 36-pin, 0.25-in.-sq. post in double row right-angle shroud strip on 0.100 centers. #BST–118–09–G–D–318–RA	J6	1BB1

QTY	Item and Manufacturer	Designation	Board Location
1	Rear Bracket. Globe Mfg, #G01 (basic blank) bracket. (modified at NRaD)		
1	Nylon 6–32 3/4-in. machine screw for U40	U40	1DD1
1	Nylon 6–32 nut for machine screw for U40	U40	1DD1
1	Insulator for U40. Wakefield #175–6–240P. Kapton insulator for type 270 AB heat sink	U40	1DD1

APPENDIX 3-A

The appendix compares the first volumetric interface board, Volumetric #1, and its successor, Volumetric #2, in detail on the first four pages.

Next are circuit diagrams for the Volumetric #2 Electronic PC Control Card. Notations contained in rectangular boxes refer to the signal entering or leaving the drawing. Designators such as (7A3) refer to sheet 7, Row A, Column 3.

The last two diagrams show component physical locations. Parts with designators such as 1AA7 refer to layer 1, the front layer of the 10-layer board, and AA7 refers to Row AA, Column 7. The prefix 10 refers to the tenth layer or the back side, example: 10BB5.

Signal flow is predominantly from drawing 1 left to right, sheet 1 to sheet 7, with the computer interface starting on the left of drawing 1. Analog and digital outputs end on the right side of sheet 7. Signals preceded by * indicate that the signal is low true and can be read as NOT(XXX). Triangles containing a D indicate digital ground and those with an A indicate analog ground.

There are numerous test points marked TP # as well as similar connections marked P # and E #; some may contain jumpers described in section 2.

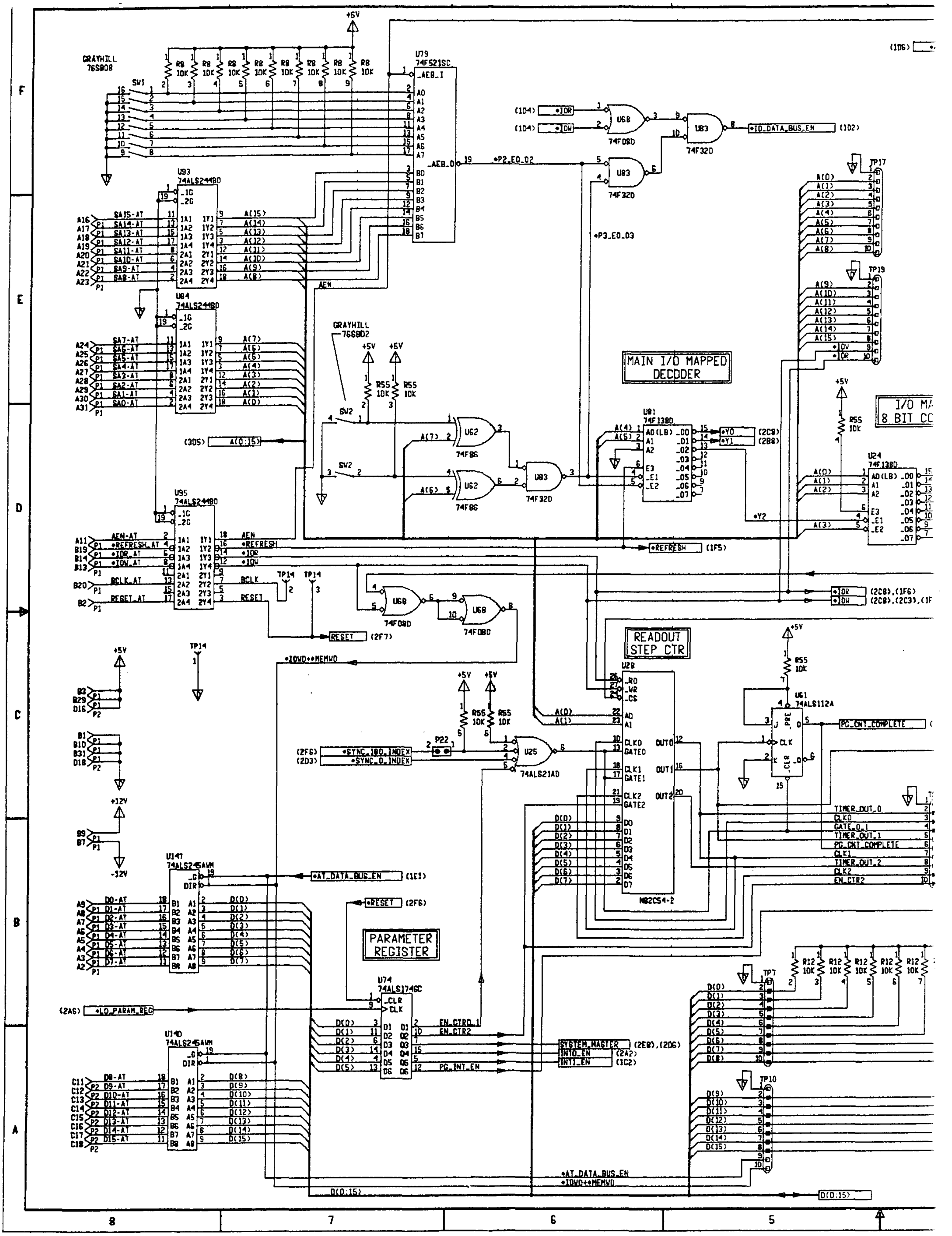
A functional comparison of the first- and second-generation interface cards is described below.

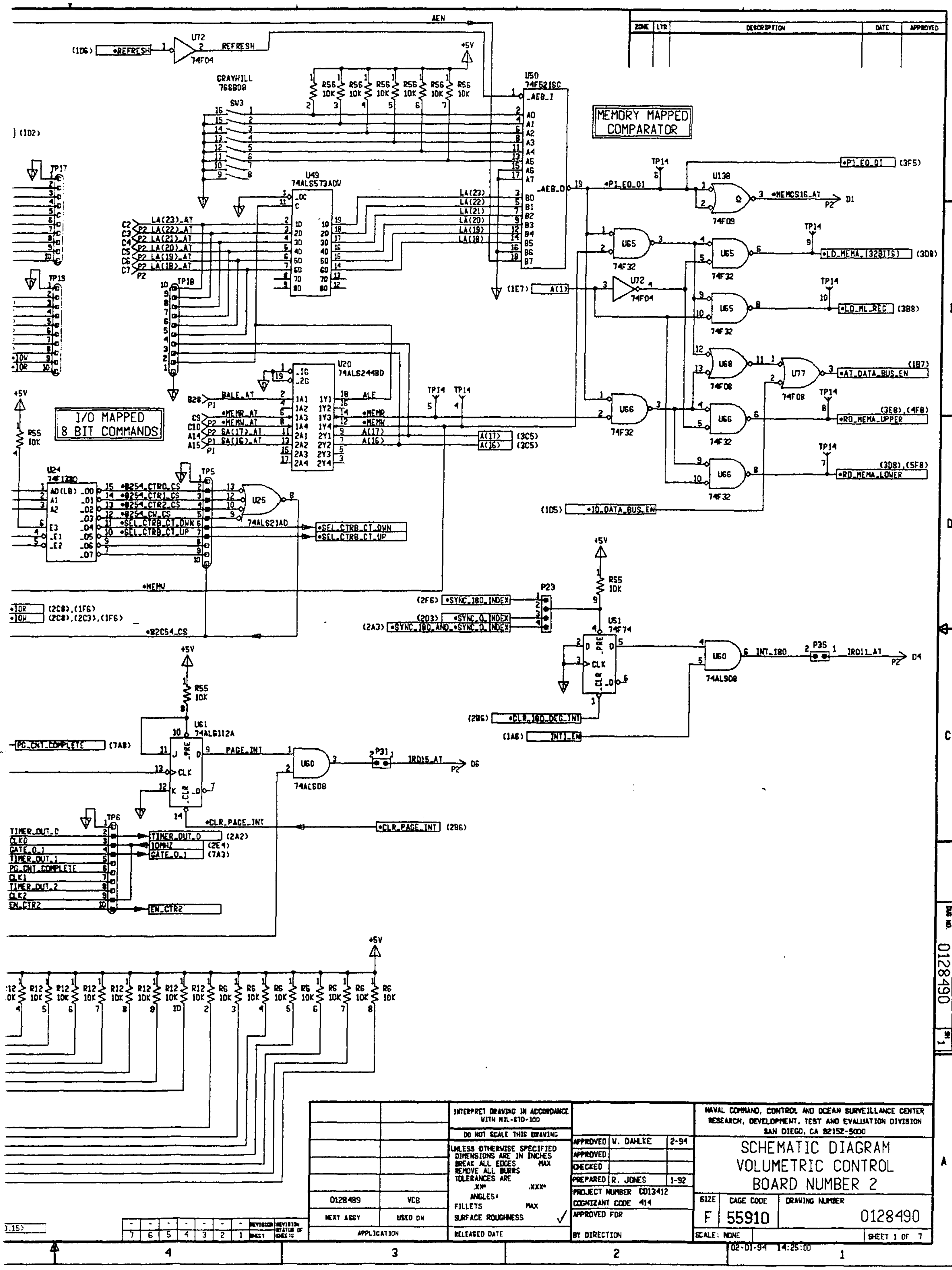
	Volumetric #1	Volumetric #2
Memory Capacity	12,288—24-bit Voxel Words in Dual-Port RAM.	65,536—32-bit Voxel Words in Dual-Port RAM.
Memory Word Structure	X – 9 bits Y – 9 bits I – 4 bits	X – 12 bits Y – 12 bits I – 8 bits
	Extended Video – 1 bit	X11 position is either X11 (MSB) or Extended Video.
	Spare – 1 bit	Y11 position is either Y11 (MSB) or Full Width Video.
Port A RAM Address	Input/Output Space.	Direct Memory Mapped. 256-KByte Address Block in 1-Meg to 16-Meg Address Range.
Control Commands	Input/Output Mapped.	Input/Output Mapped
Programmable Timer Clock	8 MHz (125-ns Period).	10 MHz (100-ns Period).
Maximum Voxel Output Rate	4 Million Voxels per second.	5 Million Voxels per second.

	Volumetric #1	Volumetric #2
Video Lookup Table RAM	None, Hard-Wired	8 Different 256-bit pages 8 bits wide.
X Analog Output	None	Via 4K x 12 "X" EEPROM resolution table. (–5 V into 50-ohm Load Max)
Y Analog Output	None	Via 4K x 12 "Y" EEPROM resolution table. (–5 V into 50 Ohm Load Max)
I Analog	16 Levels, (0 to +1 V Max) into 50 ohms. Blanking = 0 V.	256 Levels, (0 to +1 V Max) into 50 ohms. Blanking = 0 V.
X Digital	9 bits Max to NEOS.	12 bits Max to NEOS.
Y Digital	9 bits Max to NEOS.	12 bits Max to NEOS.
I Digital	None	8 bits to NEOS.
Index "A"	None	Pulse occurs on Initial Voxel "A" readout and every 4th DLY_CLK pulse thereafter. Available on J6.
BUF–DLY–CLKB	Internal Only.	Buffered Clock "B", Mem B Read-Out Clock. Available on J6.
Computer Interrupts	1 – Int 0 or Int 180	3 – Int 0, Int 180, End of Page Int.
Schematics	4 – "D" Sized Dwgs	7 – "D" Sized Dwgs
Board Type	IBM "AT", 8 Layers, 8-Mil Traces with 8-Mil Separation.	IBM "AT", 10 Layers, 7-Mil Traces with 6-Mil Separation.
General Information	309 Components, 2162 Wires, 548 Nets, 1240 Vias (30 Mil with 15-Mil Hole), 1-ounce Cu wires.	448 Components, 4255 Wires, 758 Nets, 2775 Vias (30 Mil with 15-Mil Hole), 1-ounce Cu wires.
E–Motor Output	Digital 12 bits converted to Analog Voltage (0 V to +10 V) to control Helix DC Motor. **Note**: Maximum Motor Voltage currently adjusted to +10 V.	Digital 12 bits converted to Analog Voltage (0 V to +10 V) to control Helix DC Motor. **Note**: Maximum Motor Voltage currently adjusted to +5 V.

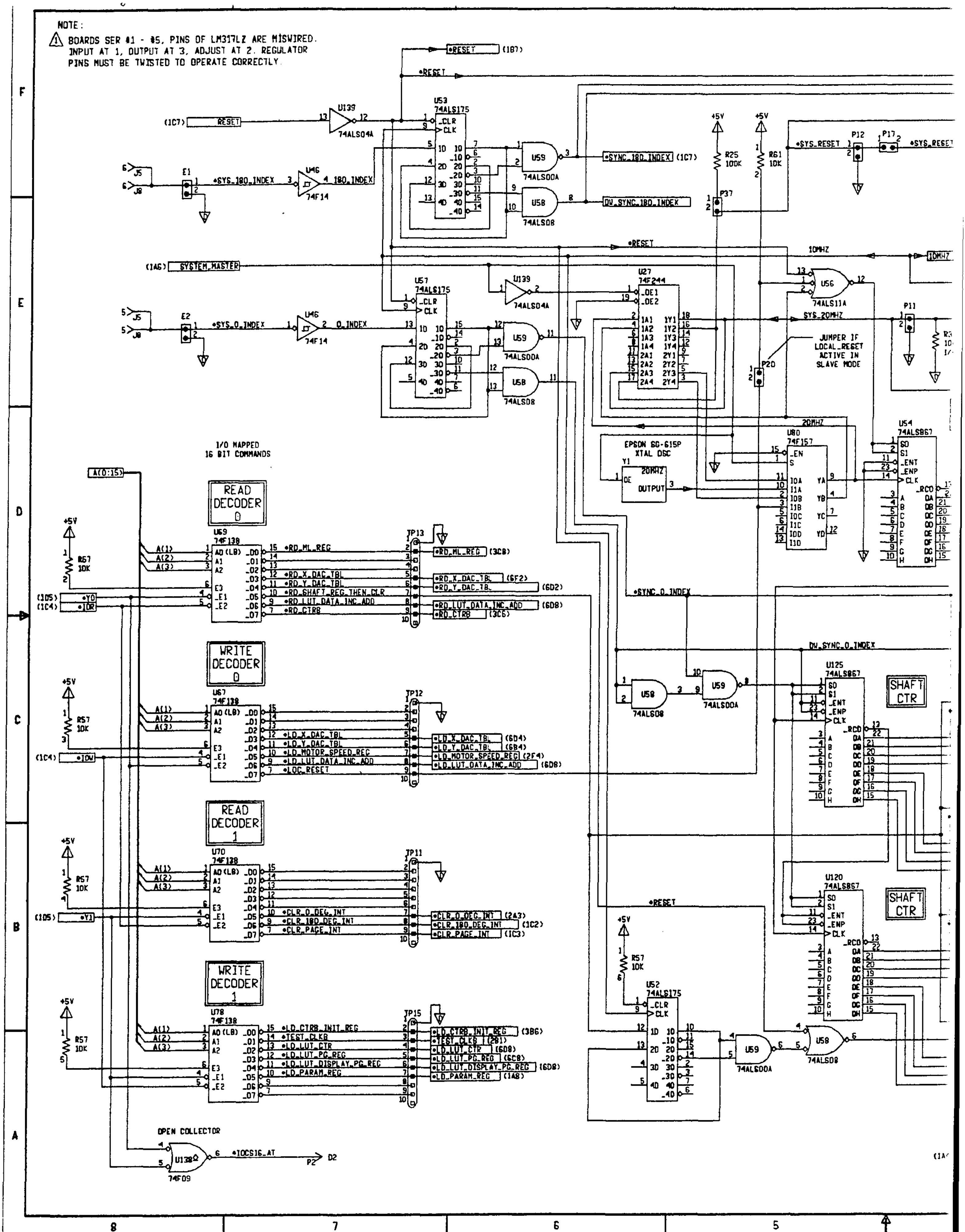
	Volumetric #1	Volumetric #2
Motor Shaft's Actual Speed	Shaft Counter counts Internal 250-kHz Clks between *System 0 Index pulses. The previous count value is transferred to the Shaft Reg at the *Sync 0 Index low-to-high transition and is available to be read by the computer for one shaft revolution. **Note**: The Shaft Register is cleared whenever the computer reads its contents.	Shaft Counter counts Internal 312.5-kHz Clks between *System 0 Index pulses. The previous count value is transferred to the Shaft Reg at the *Sync 0 Index low-to-high transition and is available to be read by the computer for one shaft revolution. **Note**: The Shaft Register is cleared whenever the computer reads its contents.
Memory B Readout	Nominally Increments CtrB in the Helix Mode. CtrB reverses its counting direction on each Index pulse in the Piston Mode of operation.	Nominally Increments CtrB in the Helix Mode. CtrB reverses its counting direction on each Index pulse in the Piston Mode of operation.
Intensity Delay	Delay for a fixed period equal to T (Optical Access Time) at the start of each voxel. T = Optical Beam Diam/ Acoustic Velocity = 10.3 microseconds for the 256 by 256—25-MHz NEOS Green Scanner.	Delay for a fixed period equal to T (Optical Access Time) at the start of each voxel.
Intensity Modes	PW – Fixed Pulse Width Video after initial blanking delay. Extended Video – Extends PW Video level to the beginning of the next voxel. Full Width Video Option not available. Overlap Video Option not available.	PW – Fixed Pulse Width Video after initial blanking delay. Extended Video – Extends PW Video level to the beginning of the next voxel. Full Width Video – Full Video without blanking over the next voxel period. Overlap Video – Old Voxel's video overlaps into the initial blanking of the Next Voxel to utilize the Old acoustic wave still in the Acousto Optic Crystals.

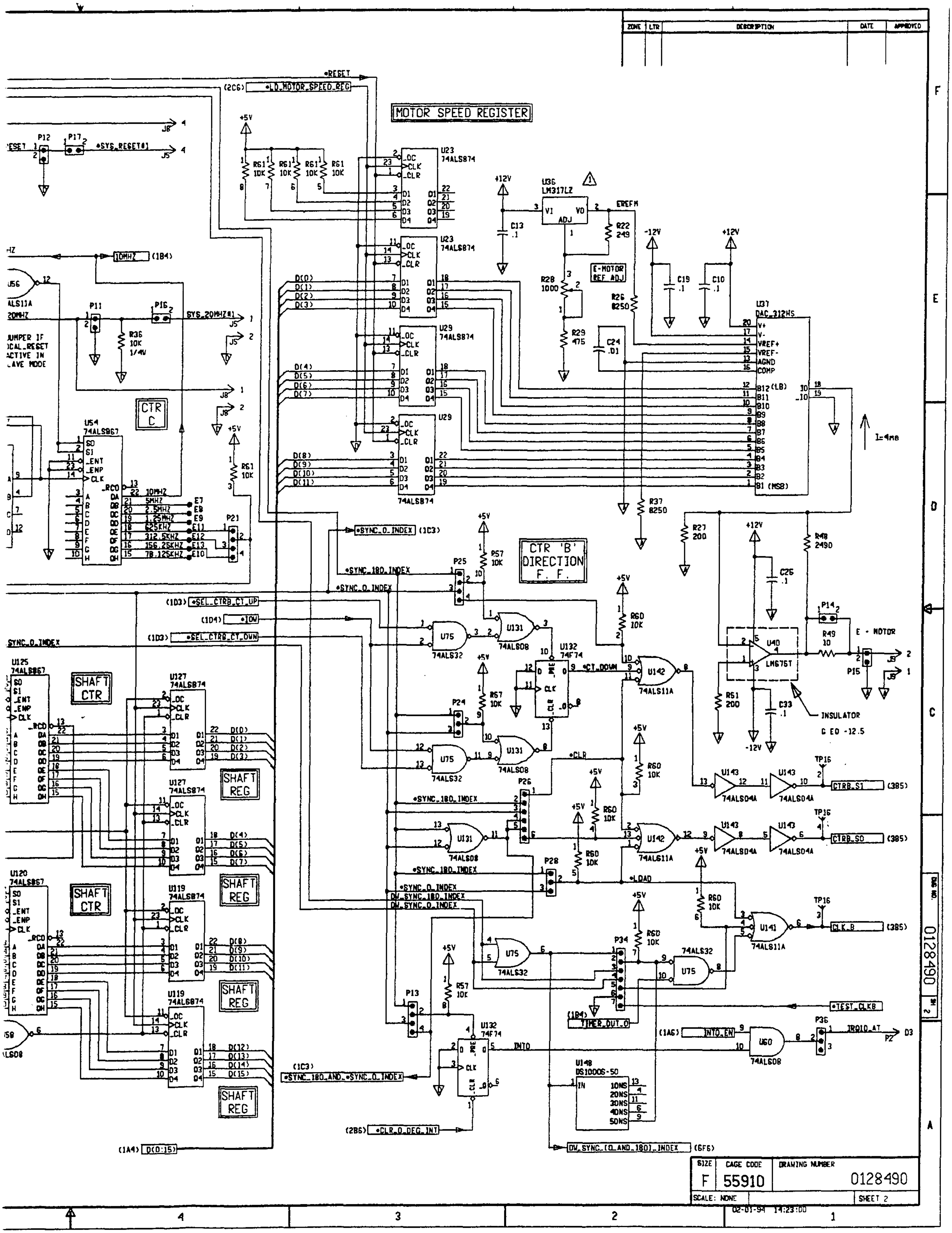
	Volumetric #1	Volumetric #2
Multiple Cards for Color	Each Board controls a different colored laser beam. One card is Master and synchronizes the other Slave cards.	Each Board controls a different colored laser beam. One card is Master and synchronizes the other Slave cards.
Power	+5 V. 10. 29 watts +12 V –12 V	19.78 watts

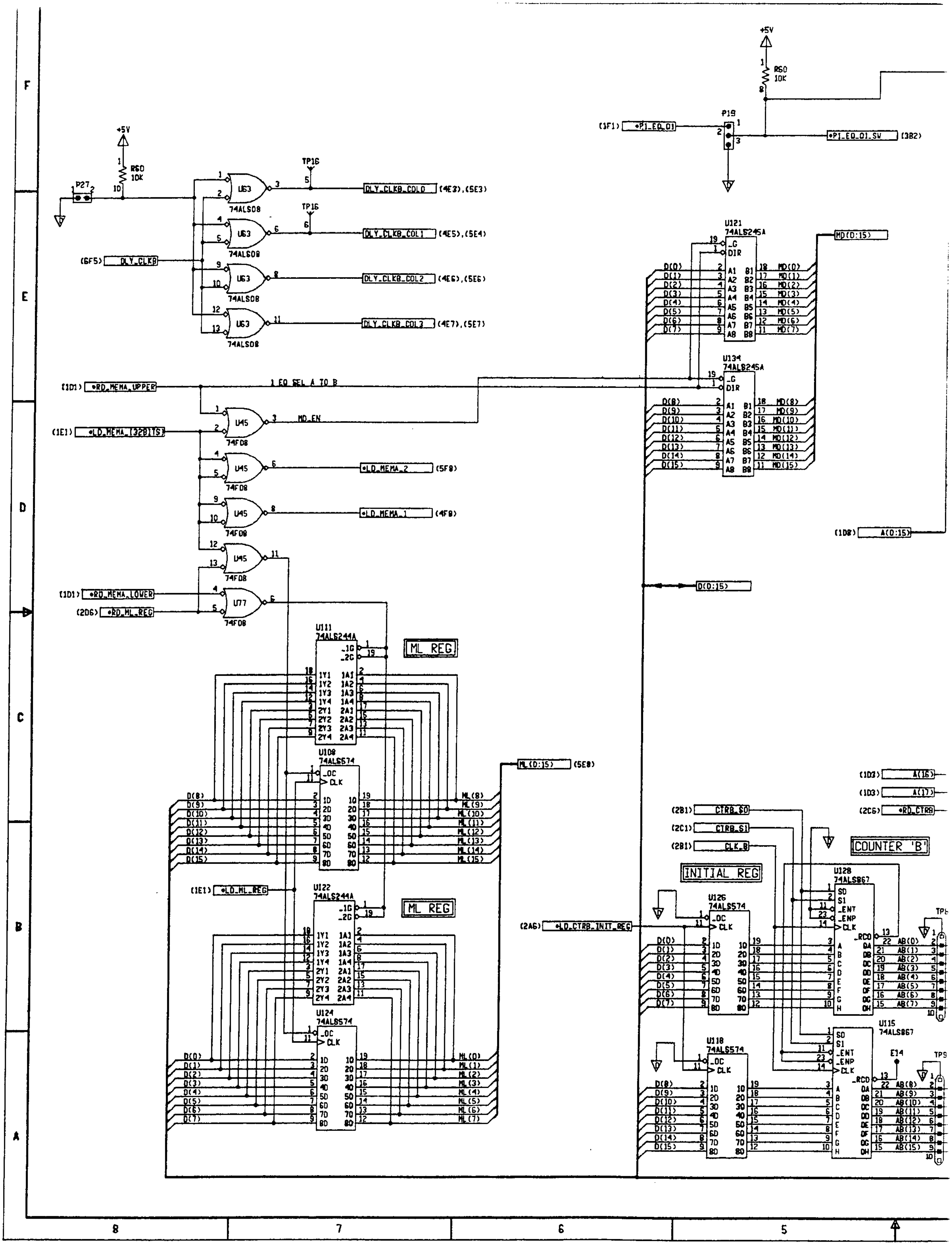

MAIN I/O MAPPED DECODER
READOUT STEP CTR
PARAMETER REGISTER
I/O MA
8 BIT CC
GRAYHILL 76SB08
GRAYHILL 76SB02
U79 74F521SC
U93 74ALS244BD
U94 74ALS244BD
U95 74ALS244BD
U68 74F08D
U83 74F32D
U62 74F86
U81 74F138D
U24 74F138D
U28 N82C54-2
U61 74ALS112A
U25 74ALS21AD
U74 74ALS174SC
U147 74ALS245AWM
U140 74ALS245AWM
*IO_DATA_BUS_EN
*REFRESH
*IOR
*IOW
RESET
*IOWD+*MEMWD
*SYNC_180_INDEX
*SYNC_0_INDEX
*AT_DATA_BUS_EN
*LD_PARAM_REG
SYSTEM_MASTER
INTO_EN
INT1_EN
PG_CNT_COMPLETE
TIMER_OUT_0
CLK0
GATE_0_1
TIMER_OUT_1
CLK1
TIMER_OUT_2
CLK2
EN_CTR2
A(0:15)
D(0:15)
8
7
6
5



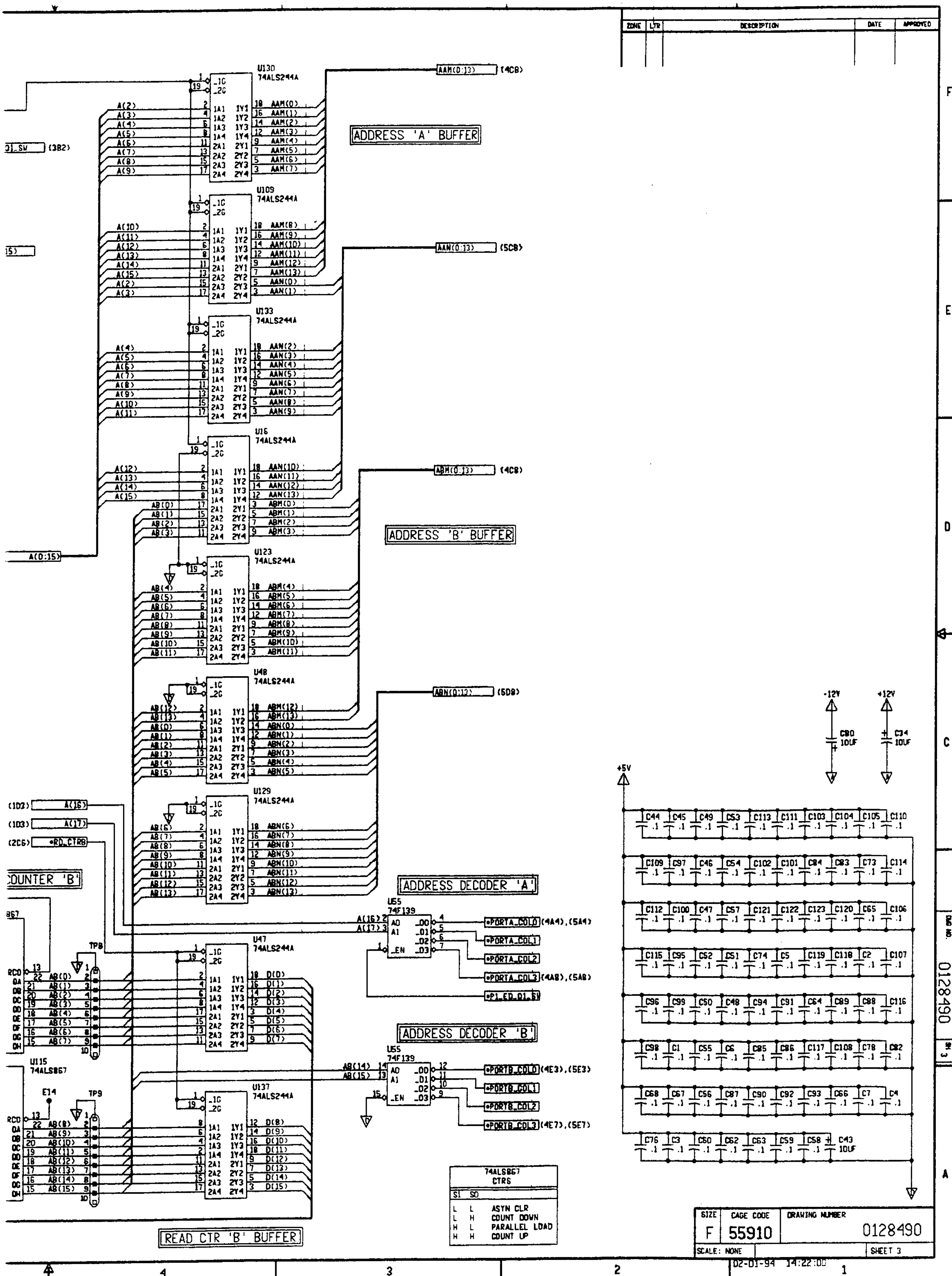
MEMORY MAPPED COMPARATOR
I/O MAPPED 8 BIT COMMANDS
GRAYHILL 76SB08
U50 74F521SC
U49 74ALS573ADW
U20 74ALS244BD
U24 74F138D
U25 74ALS21AD
U51 74F74
U61 74ALS112A
U60 74ALS08
U138 74F09
U65 74F32
U66 74F32
U68 74F08
U77 74F08
U72 74F04
INTERPRET DRAWING IN ACCORDANCE WITH MIL-STD-100
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
BREAK ALL EDGES MAX
REMOVE ALL BURRS
TOLERANCES ARE
ANGLES
FILLETS MAX
SURFACE ROUGHNESS
RELEASED DATE
0128489
VCB
NEXT ASSY
USED ON
APPLICATION
APPROVED W. DAHLKE 2-94
APPROVED
CHECKED
PREPARED R. JONES 1-92
PROJECT NUMBER CD13412
COGNIZANT CODE 414
APPROVED FOR
BY DIRECTION
NAVAL COMMAND, CONTROL AND OCEAN SURVEILLANCE CENTER
RESEARCH, DEVELOPMENT, TEST AND EVALUATION DIVISION
SAN DIEGO, CA 92152-5000
SCHEMATIC DIAGRAM
VOLUMETRIC CONTROL
BOARD NUMBER 2
SIZE F
CAGE CODE 55910
DRAWING NUMBER 0128490
SCALE: NONE
SHEET 1 OF 7
02-01-94 14:25:00

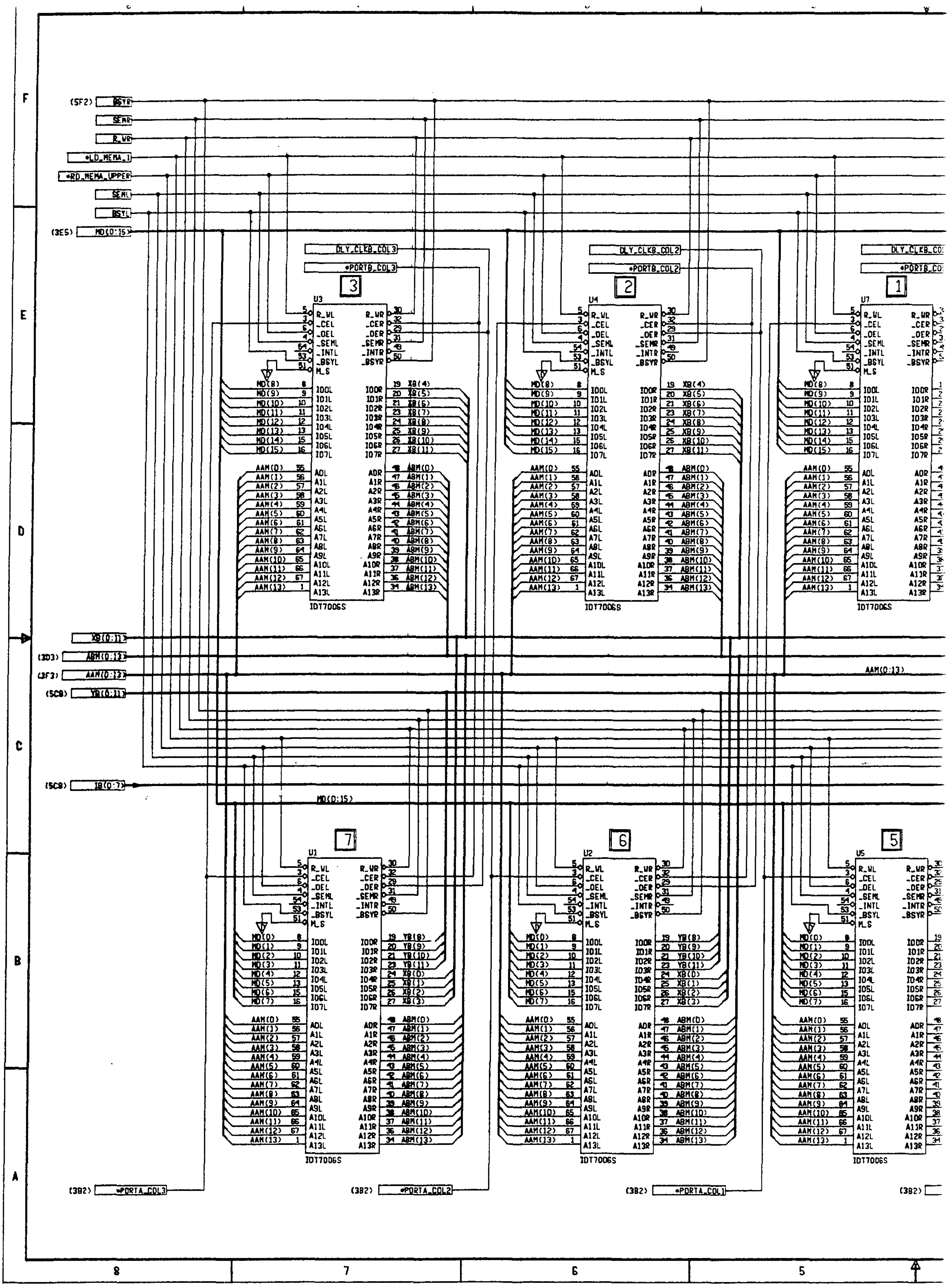

NOTE:
BOARDS SER #1 - #5, PINS OF LM317LZ ARE MISWIRED.
INPUT AT 1, OUTPUT AT 3, ADJUST AT 2. REGULATOR
PINS MUST BE TWISTED TO OPERATE CORRECTLY.
*RESET (1B7)
*RESET
(1C7) RESET
U139 74ALS04A
U53 74ALS175
U59 74ALS00A
U58 74ALS08
*SYNC_180_INDEX (1C7)
DV_SYNC_180_INDEX
*SYS_180_INDEX
180_INDEX
U46 74F14
E1
J5
J8
+5V
R25 100K
R61 10K
P37
P12
P17
*SYS_RESET
(1A6) SYSTEM_MASTER
10MHZ
U57 74ALS175
U27 74F244
U56 74ALS11A
P11
SYS_20MHZ
JUMPER IF LOCAL_RESET ACTIVE IN SLAVE MODE
P20
E2
*SYS_0_INDEX
0_INDEX
EPSON SG-615P XTAL OSC
Y1 20MHZ OUTPUT
U80 74F157
20MHZ
U54 74ALS867
I/O MAPPED
16 BIT COMMANDS
A(0:15)
READ DECODER 0
U69 74F138
R57 10K
TP13
*RD_ML_REG (3C8)
*RD_X_DAC_TBL (6F2)
*RD_Y_DAC_TBL (6D2)
*RD_SHAFT_REG_THEN_CLR
*RD_LUT_DATA_INC_ADD (6D8)
*RD_CTRB (3C6)
(1D5) *Y0
(1C4) *IOR
*SYNC_0_INDEX
DV_SYNC_0_INDEX
U125 74ALS867
SHAFT CTR
WRITE DECODER 0
U67 74F138
TP12
*LD_X_DAC_TBL (6D4)
*LD_Y_DAC_TBL (6B4)
*LD_MOTOR_SPEED_REG (2F4)
*LD_LUT_DATA_INC_ADD (6D8)
*LOC_RESET
(1C4) *IOW
READ DECODER 1
U70 74F138
TP11
*CLR_0_DEG_INT (2A3)
*CLR_180_DEG_INT (1C2)
*CLR_PAGE_INT (1C3)
(1D5) *Y1
U120 74ALS867
SHAFT CTR
WRITE DECODER 1
U78 74F138
TP15
*LD_CTRB_INIT_REG (3B6)
*TEST_CLKB (2B1)
*LD_LUT_CTR (6D8)
*LD_LUT_PG_REG (6C8)
*LD_LUT_DISPLAY_PG_REG (6D8)
*LD_PARAM_REG (1A8)
U52 74ALS175
OPEN COLLECTOR
U138 74F09
*IOCS16_AT
P2 D2
F
E
D
C
B
A
8
7
6
5


MOTOR SPEED REGISTER
CTR 'B' DIRECTION F. F.
SHAFT CTR
SHAFT REG
CTR C
E-MOTOR REF ADJ
INSULATOR
E - MOTOR
SIZE F
CAGE CODE 55910
DRAWING NUMBER 0128490
SCALE: NONE
SHEET 2

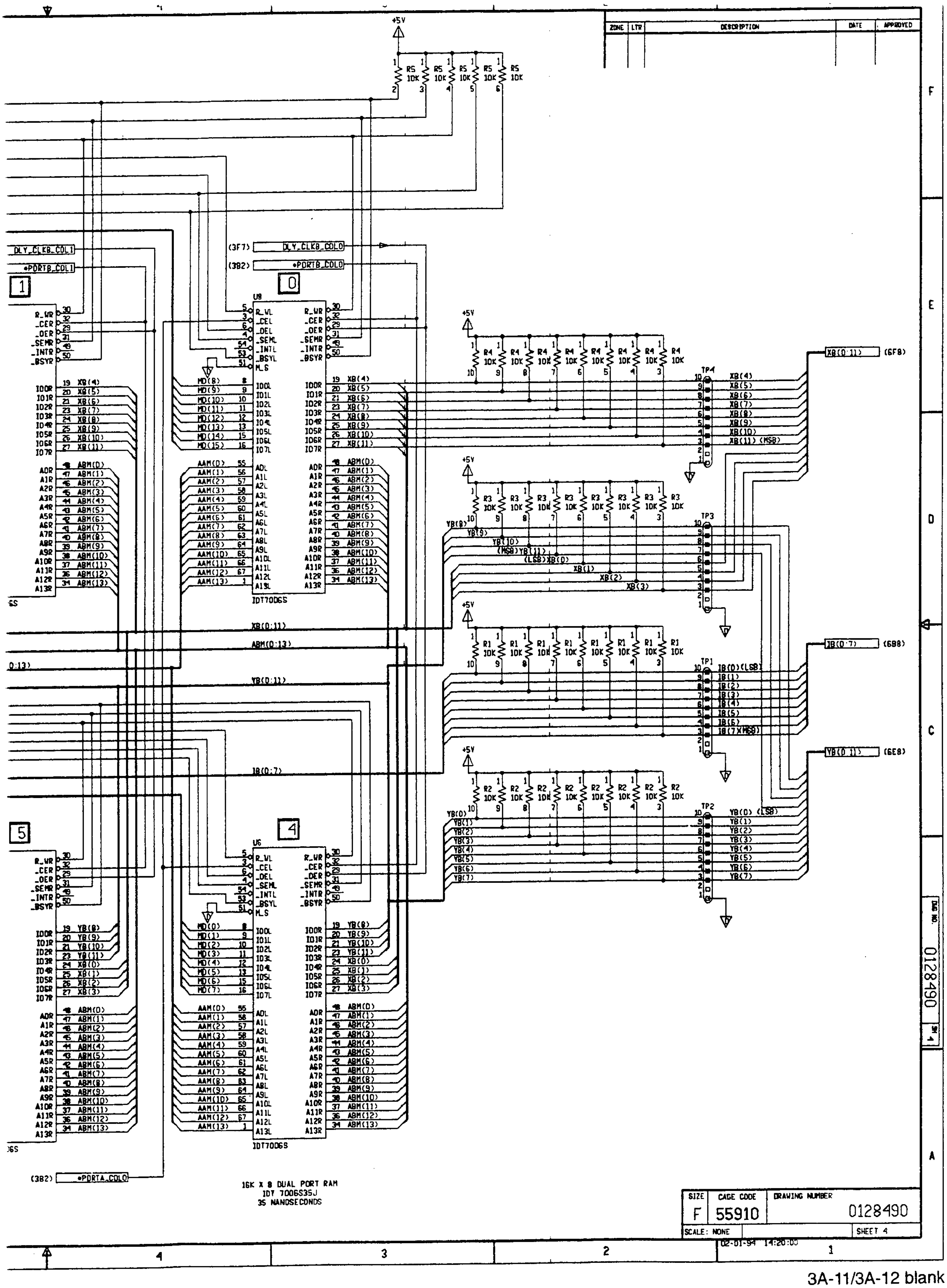


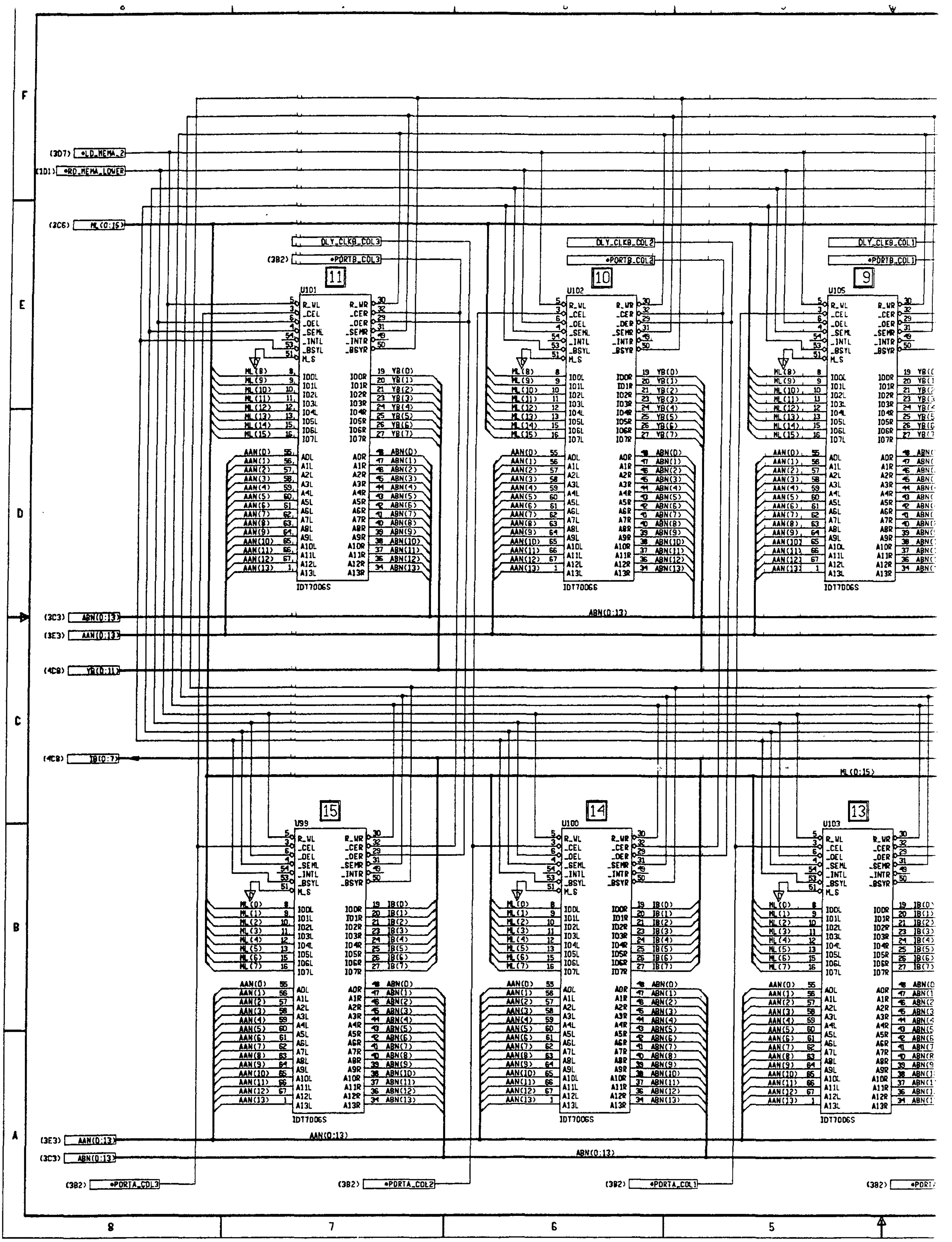
ML REG
ML REG
INITIAL REG
COUNTER 'B'
1 EQ SEL A TO B
MD_EN
DLY_CLKB
DLY_CLKB_COL0
DLY_CLKB_COL1
DLY_CLKB_COL2
DLY_CLKB_COL3
*RD_MEMA_UPPER
*LD_MEMA_[32BITS]
*LD_MEMA_2
*LD_MEMA_1
*RD_MEMA_LOWER
*RD_ML_REG
*LD_ML_REG
*LD_CTRB_INIT_REG
*P1_EQ_01
*P1_EQ_01_SW
MD(0:15)
A(0:15)
D(0:15)
ML(0:15)
CTRB_S0
CTRB_S1
CLK_B
*RD_CTRB
U111 74ALS244A
U122 74ALS244A
U108 74ALS574
U124 74ALS574
U121 74ALS245A
U134 74ALS245A
U126 74ALS574
U118 74ALS574
U128 74ALS867
U115 74ALS867
U63 74ALS08
U45 74F08
U77 74F08
R60 10K
+5V
P27
P19
TP16
E14
F
E
D
C
B
A
8
7
6
5


ADDRESS 'A' BUFFER
ADDRESS 'B' BUFFER
ADDRESS DECODER 'A'
ADDRESS DECODER 'B'
READ CTR 'B' BUFFER
U130 74ALS244A
U109 74ALS244A
U133 74ALS244A
U16 74ALS244A
U123 74ALS244A
U48 74ALS244A
U129 74ALS244A
U47 74ALS244A
U137 74ALS244A
U115 74ALS867
U55 74F139
AAM(0:13) (4C8)
AAN(0:13) (5C8)
ABM(0:13) (4C8)
ABN(0:13) (5D8)
A(0:15)
PORTA_COL0 (4A4),(5A4)
PORTA_COL1
PORTA_COL2
PORTA_COL3 (4A8),(5A8)
P1_ED_D1_SW
PORTB_COL0 (4E3),(5E3)
PORTB_COL1
PORTB_COL2
PORTB_COL3 (4E7),(5E7)
TP8
TP9
E14
+5V
-12V
+12V
C80 10UF
C34 10UF
C43 10UF
74ALS867 CTRS
S1 S0
L L ASYN CLR
L H COUNT DOWN
H L PARALLEL LOAD
H H COUNT UP
ZONE LTR DESCRIPTION DATE APPROVED
SIZE F
CAGE CODE 55910
DRAWING NUMBER 0128490
SCALE: NONE
SHEET 3
02-01-94 14:22:00
4 3 2 1
F E D C A

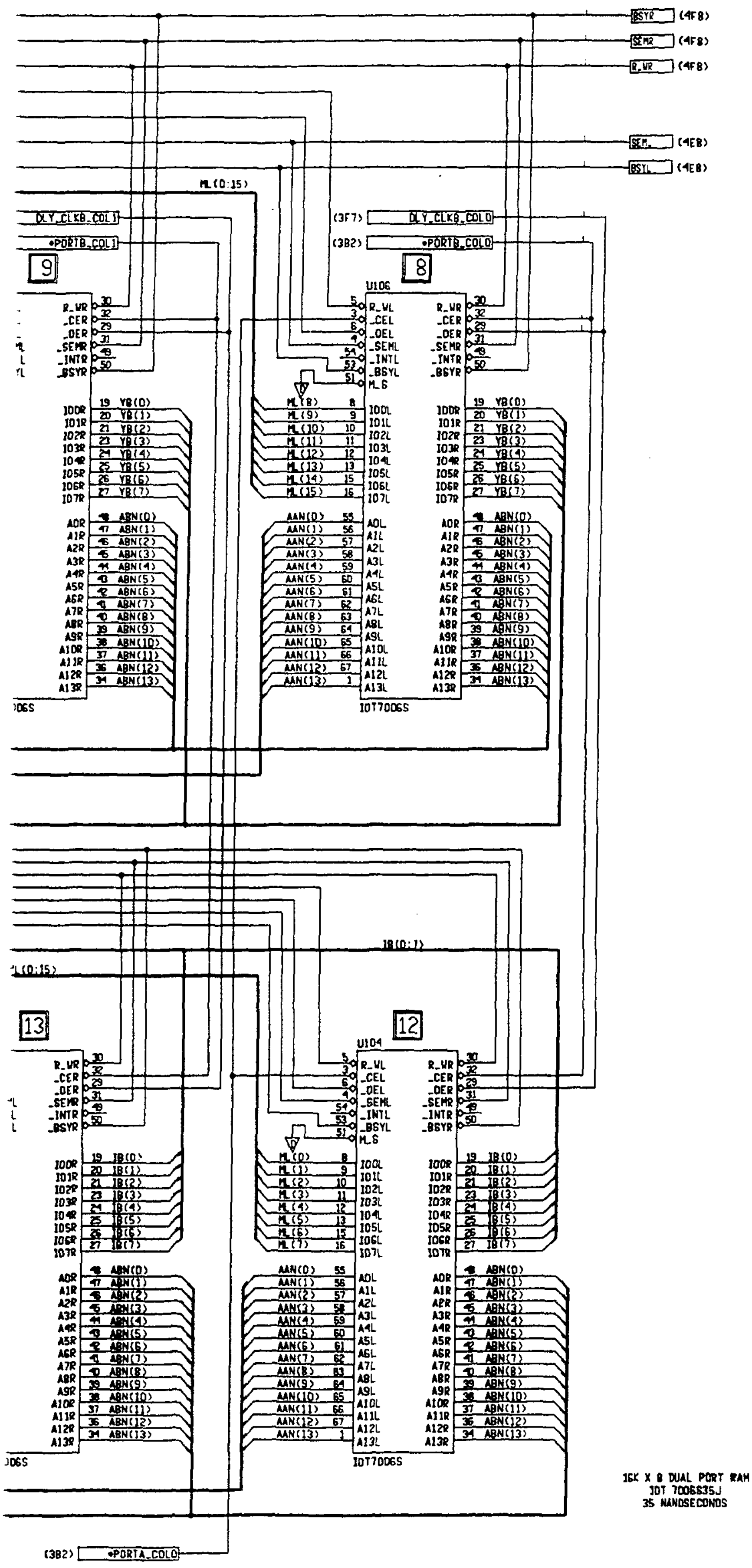


F
E
D
C
B
A
(5F2) BSYR
SEMR
R_WR
*LD_MEMA_1
*RD_MEMA_UPPER
SEML
BSYL
(3E5) MD(0:15)
DLY_CLKB_COL3
*PORTB_COL3
DLY_CLKB_COL2
*PORTB_COL2
DLY_CLKB_CO
*PORTB_CO
3
2
1
U3
U4
U7
R_WL
_CEL
_OEL
_SEML
_INTL
_BSYL
M_S
R_WR
_CER
_OER
_SEMR
_INTR
_BSYR
IO0L
IO1L
IO2L
IO3L
IO4L
IO5L
IO6L
IO7L
IO0R
IO1R
IO2R
IO3R
IO4R
IO5R
IO6R
IO7R
A0L
A13L
A0R
A13R
MD(8)
MD(15)
XB(4)
XB(11)
AAM(0)
AAM(13)
ABM(0)
ABM(13)
IDT7006S
XB(0:11)
(3D3) ABM(0:13)
(3F3) AAM(0:13)
(5C8) YB(0:11)
AAM(0:13)
(5C8) IB(0:7)
MD(0:15)
7
6
5
U1
U2
U5
MD(0)
MD(7)
YB(8)
YB(11)
XB(0)
XB(3)
(3B2) *PORTA_COL3
(3B2) *PORTA_COL2
(3B2) *PORTA_COL1
(3B2)
8
7
6
5


ZONE
LTR
DESCRIPTION
DATE
APPROVED
+5V
R5 10K
R4 10K
R3 10K
R1 10K
R2 10K
DLY_CLKB_COL1
*PORTB_COL1
(3F7) DLY_CLKB_COL0
(3B2) *PORTB_COL0
U8
U6
IDT7006S
XB(0:11)
ABM(0:13)
YB(0:11)
IB(0:7)
TP4
TP3
TP1
TP2
XB(0:11) (6F8)
IB(0:7) (6B8)
YB(0:11) (6E8)
XB(11) (MSB)
IB(0) (LSB)
IB(7) (MSB)
YB(0) (LSB)
(3B2) *PORTA_COL0
16K X 8 DUAL PORT RAM
IDT 7006S35J
35 NANOSECONDS
SIZE F
CAGE CODE 55910
DRAWING NUMBER 0128490
SCALE: NONE
SHEET 4
02-01-94 14:20:00
DWG NO. 0128490
SH 4



(3D7) *LD_MEMA_2
(1D1) *RD_MEMA_LOWER
(2C6) ML(0:15)
DLY_CLKB_COL3
(3B2) *PORTB_COL3
DLY_CLKB_COL2
*PORTB_COL2
DLY_CLKB_COL1
*PORTB_COL1
11
U101
10
U102
9
U105
15
U99
14
U100
13
U103
R_WL
_CEL
_OEL
_SEML
_INTL
_BSYL
M_S
R_WR
_CER
_OER
_SEMR
_INTR
_BSYR
IDT7006S
ABN(0:13)
AAN(0:13)
(3C3) ABN(0:13)
(3E3) AAN(0:13)
(4C8) YB(0:11)
(4C8) IB(0:7)
ML(0:15)
(3B2) *PORTA_COL3
(3B2) *PORTA_COL2
(3B2) *PORTA_COL1
(3B2) *PORTA
8
7
6
5
F
E
D
C
B
A



16K X 8 DUAL PORT RAM
IDT 7006S35J
35 NANOSECONDS

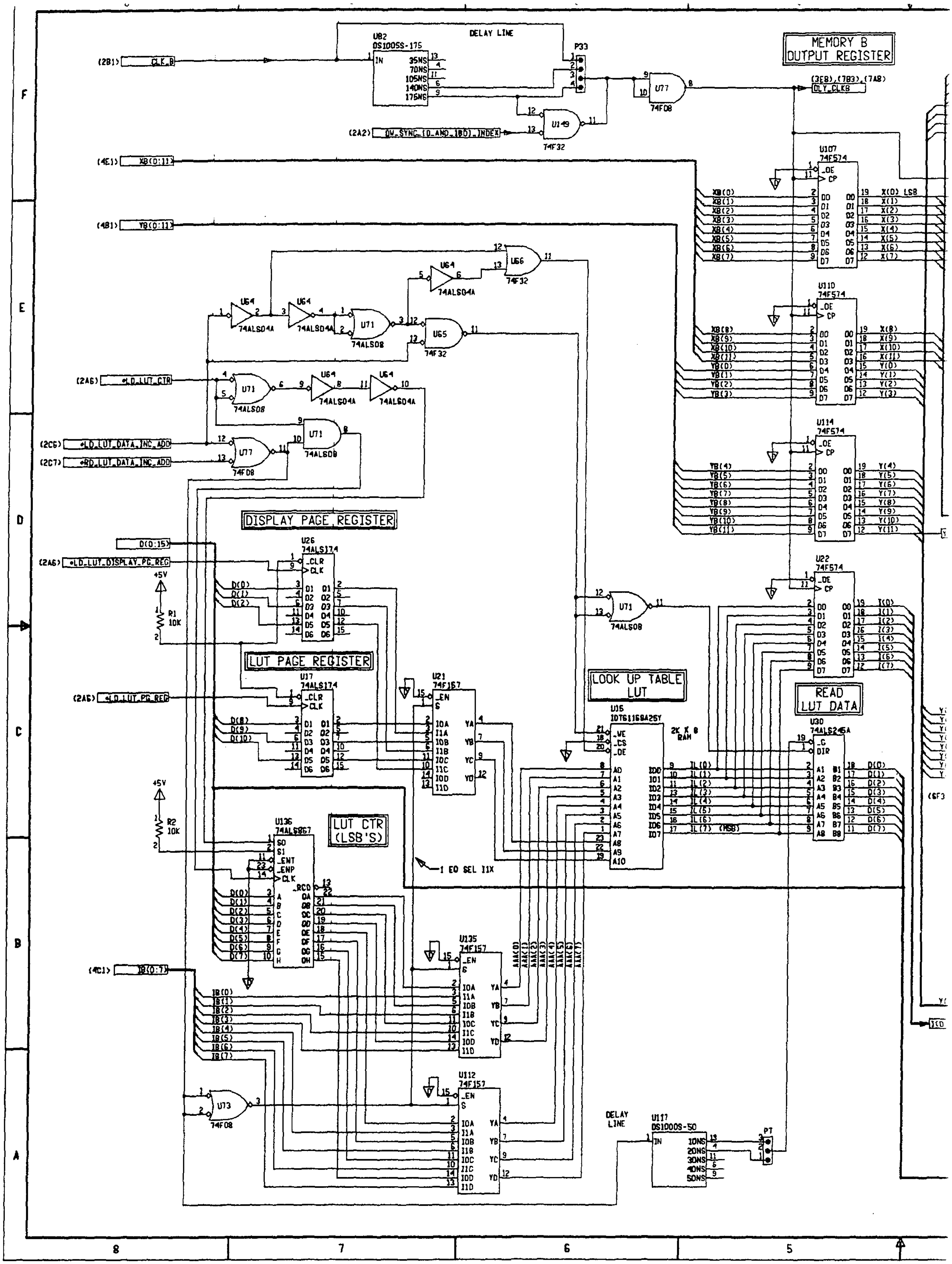
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SIZE	CAGE CODE	DRAWING NUMBER
F	55910	0128490
SCALE: NONE		SHEET 5

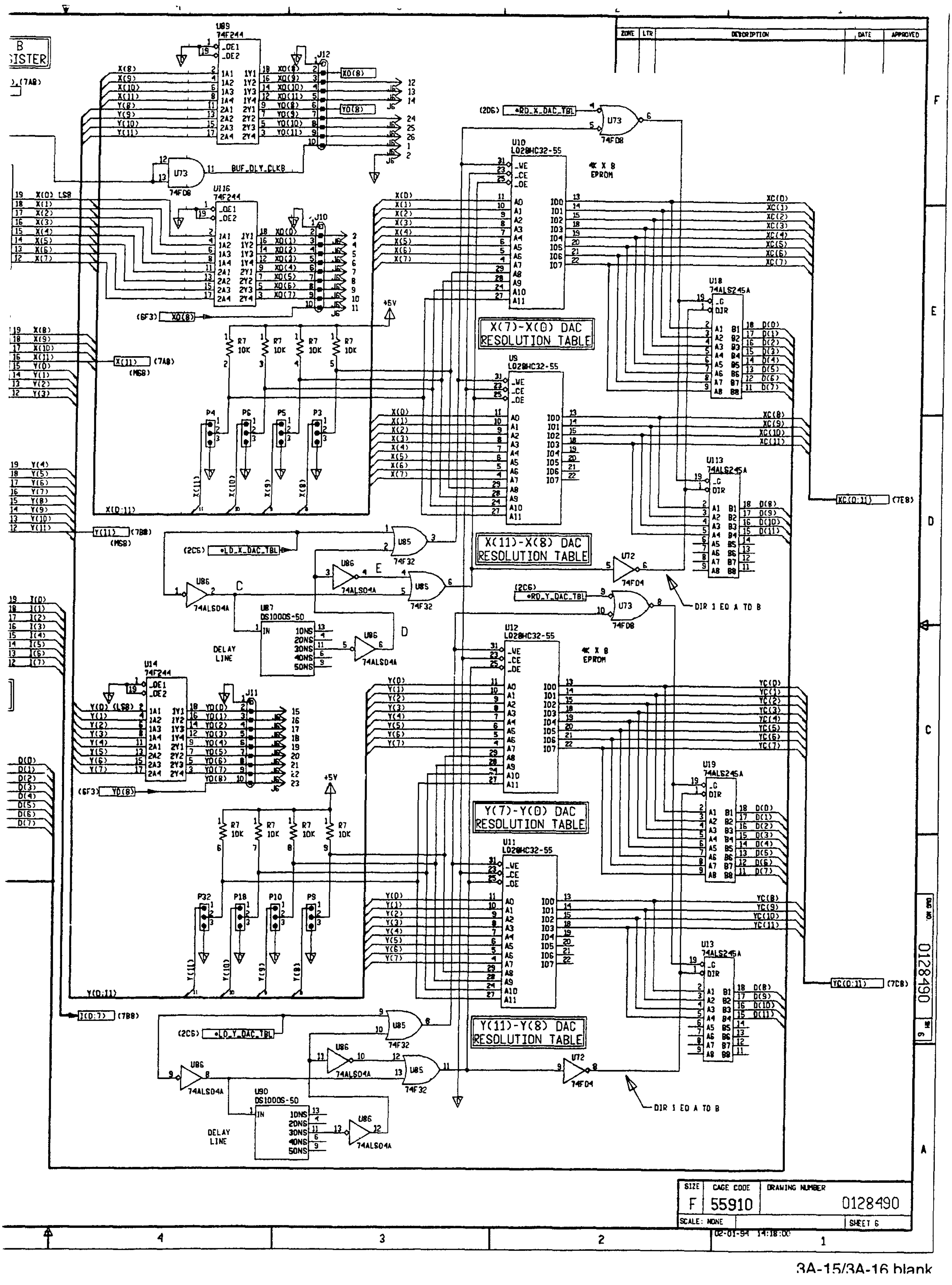
02-01-94 14:19:00

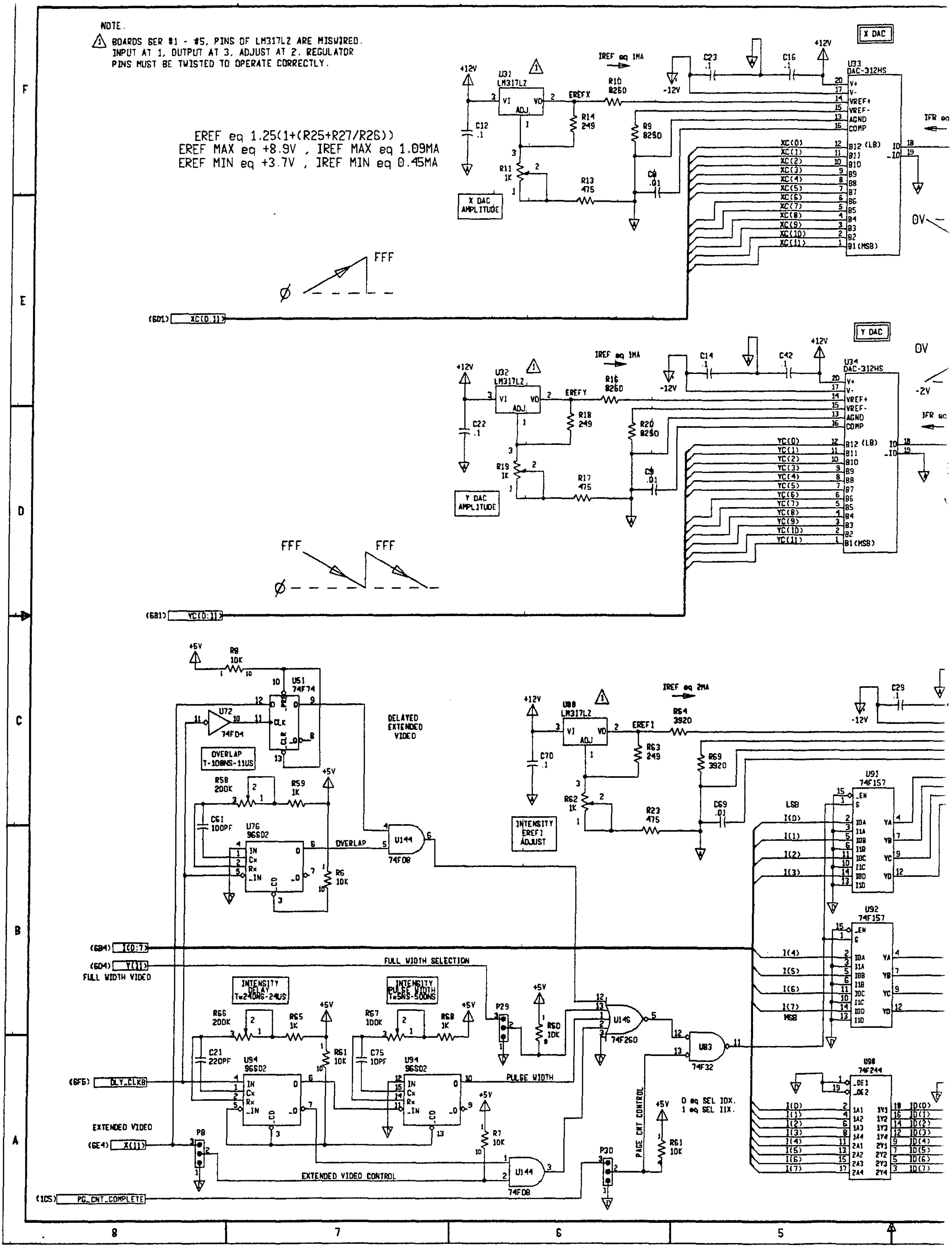
DWG NO. 0128490 SH 5

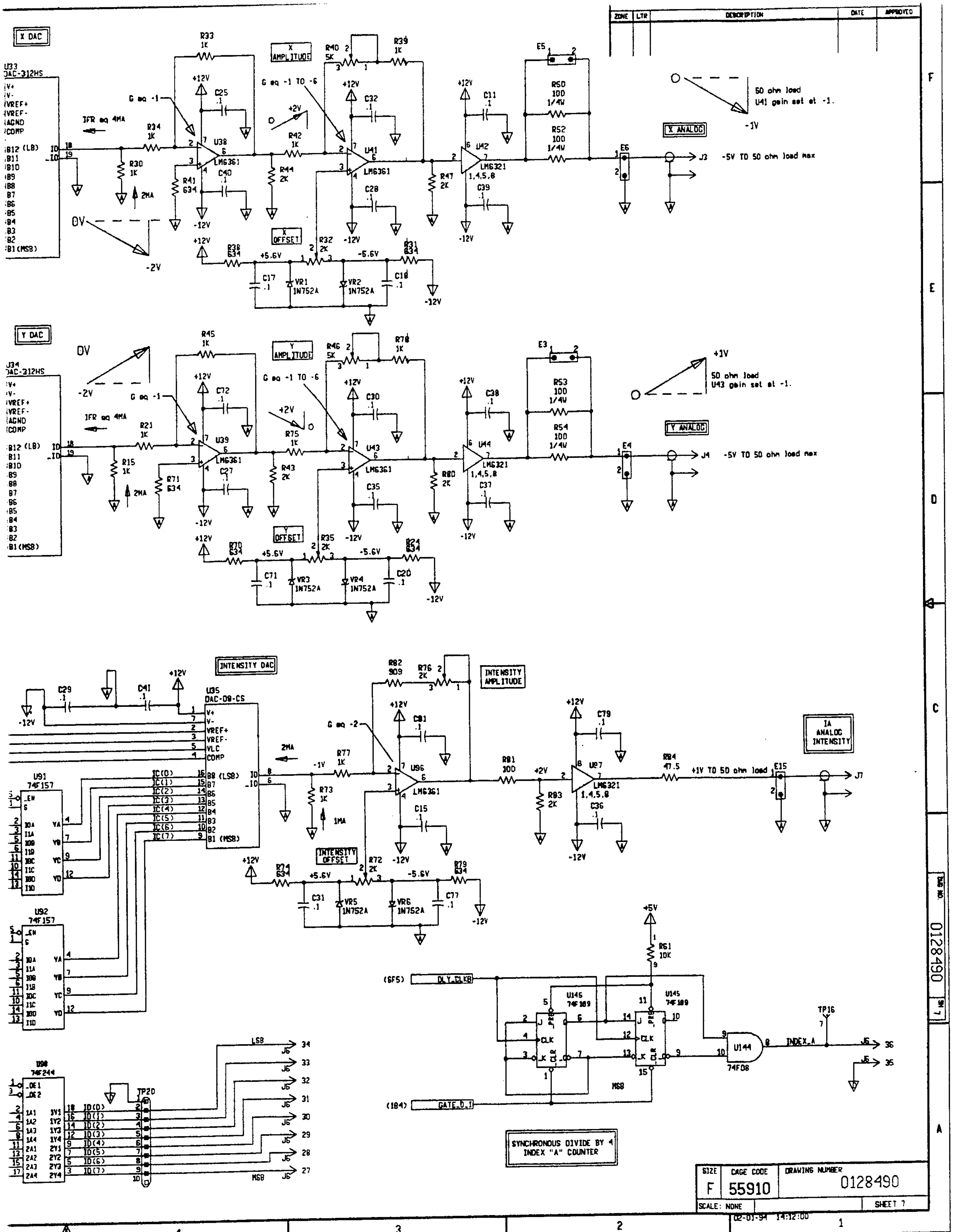
3A-13/3A-14 blank

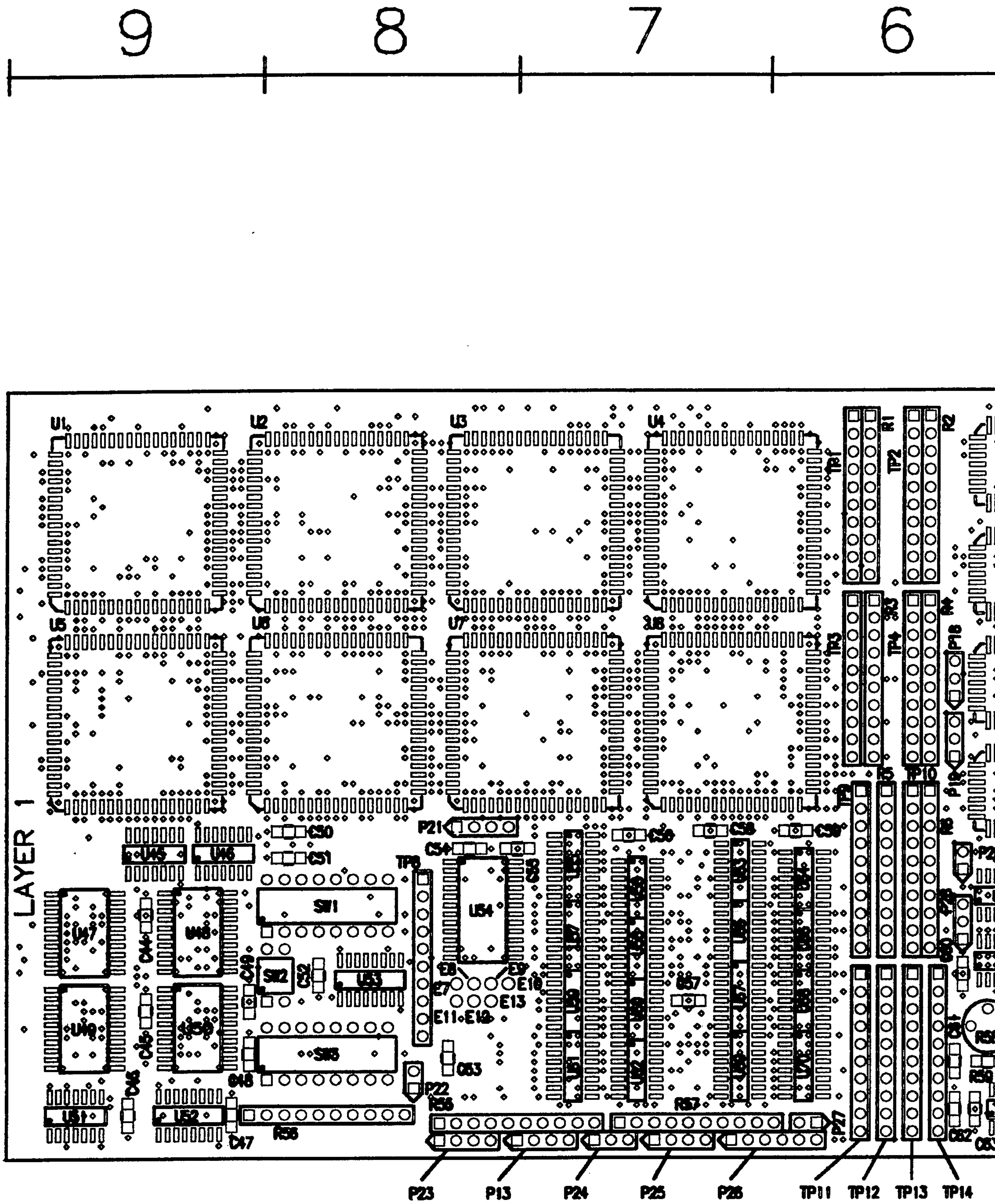


MEMORY B OUTPUT REGISTER
DELAY LINE
U82 DS1005S-175
P33
U77 74F08
U149 74F32
(2B1) CLK_B
(2A2) DV_SYNC_(0_AND_180)_INDEX
(3E8),(7B3),(7A8) DLY_CLKB
(4E1) XB(0:11)
(4B1) YB(0:11)
U107 74F574
U110 74F574
U114 74F574
U22 74F574
U64 74ALS04A
U66 74F32
U71 74ALS08
U65 74F32
(2A6) +LD_LUT_CTR
(2C6) +LD_LUT_DATA_INC_ADD
(2C7) +RD_LUT_DATA_INC_ADD
DISPLAY PAGE REGISTER
U26 74ALS174
D(0:15)
(2A6) +LD_LUT_DISPLAY_PG_REG
+5V
R1 10K
LUT PAGE REGISTER
U17 74ALS174
(2A6) +LD_LUT_PG_REG
U21 74F157
LOOK UP TABLE LUT
U15 IDT6116SA25Y
2K X 8 RAM
READ LUT DATA
U30 74ALS245A
R2 10K
U136 74ALS867
LUT CTR (LSB'S)
1 EO SEL I1X
U135 74F157
(4C1) IB(0:7)
U112 74F157
U73 74F08
DELAY LINE
U117 DS1000S-50
P7
8
7
6
5
F
E
D
C
B
A


X(7)-X(0) DAC RESOLUTION TABLE
X(11)-X(8) DAC RESOLUTION TABLE
Y(7)-Y(0) DAC RESOLUTION TABLE
Y(11)-Y(8) DAC RESOLUTION TABLE
4K X 8 EPROM
DELAY LINE
DIR 1 EQ A TO B
BUF_DLY_CLKB
*RD_X_DAC_TBL
*LD_X_DAC_TBL
*RD_Y_DAC_TBL
*LD_Y_DAC_TBL
XC(0:11) (7E8)
YC(0:11) (7C8)
I(0:7) (7B8)
SIZE F
CAGE CODE 55910
DRAWING NUMBER 0128490
SCALE: NONE
SHEET 6
02-01-94 14:18:00

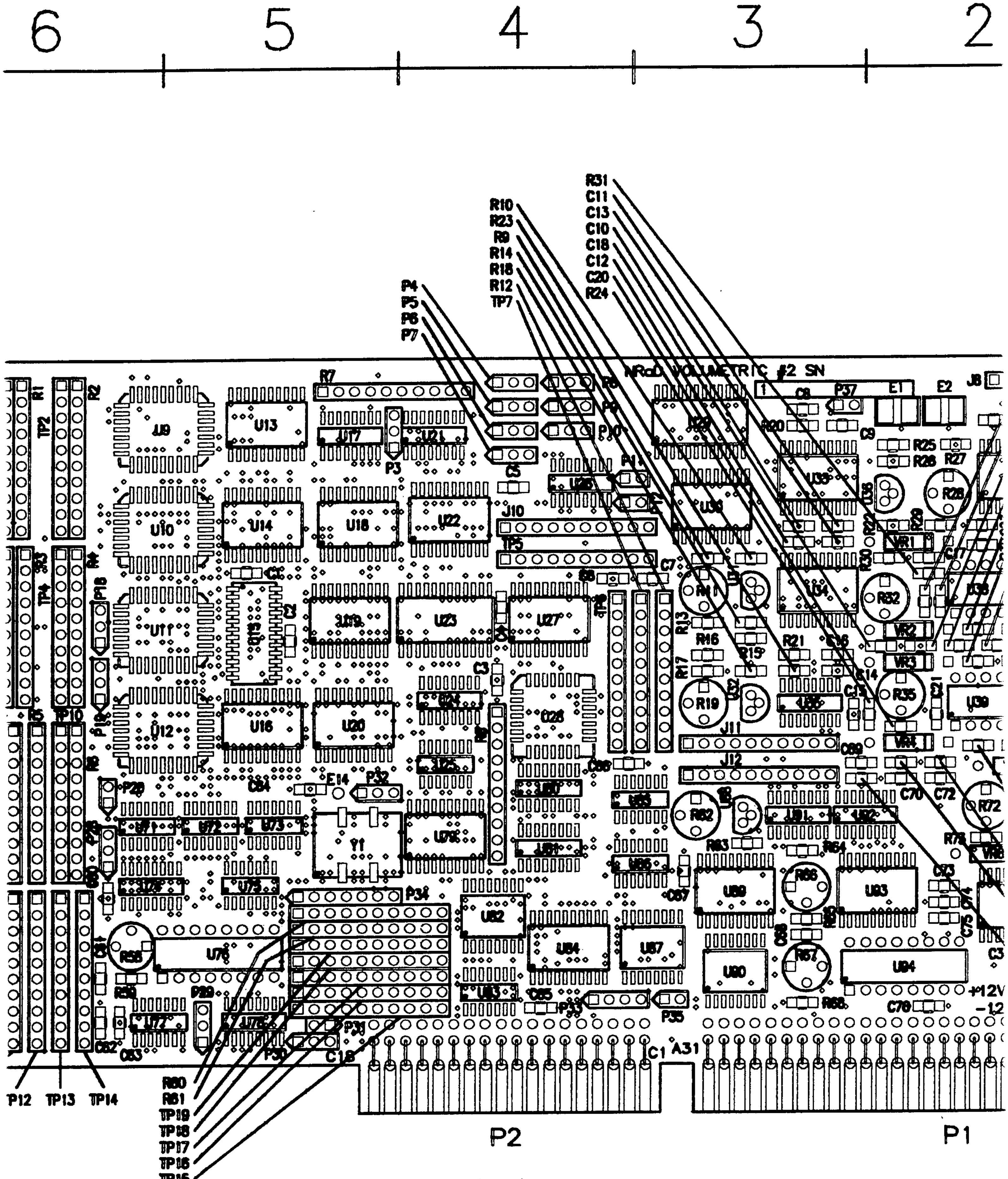

NOTE.
BOARDS SER #1 - #5, PINS OF LM317LZ ARE MISWIRED. INPUT AT 1, OUTPUT AT 3, ADJUST AT 2. REGULATOR PINS MUST BE TWISTED TO OPERATE CORRECTLY.
EREF eq 1.25(1+(R25+R27/R26))
EREF MAX eq +8.9V , IREF MAX eq 1.09MA
EREF MIN eq +3.7V , IREF MIN eq 0.45MA
X DAC
U33 DAC-312HS
Y DAC
U34 DAC-312HS
U31 LM317LZ
U32 LM317LZ
U88 LM317LZ
X DAC AMPLITUDE
Y DAC AMPLITUDE
INTENSITY EREFI ADJUST
IREF eq 1MA
IREF eq 2MA
(6D1) XC(0:11)
(6B1) YC(0:11)
FFF
DELAYED EXTENDED VIDEO
OVERLAP T=100NS-11US
OVERLAP
INTENSITY DELAY T=240NS-24US
INTENSITY PULSE WIDTH T=5NS-500NS
FULL WIDTH SELECTION
(6B4) I(0:7)
(6D4) Y(11)
FULL WIDTH VIDEO
(6F5) DLY_CLKB
EXTENDED VIDEO
(6E4) X(11)
EXTENDED VIDEO CONTROL
PULSE WIDTH
PAGE CNT CONTROL
0 eq SEL 10X.
1 eq SEL 11X.
(1C5) PG_CNT_COMPLETE
U91 74F157
U92 74F157
U98 74F244
LSB
MSB
8
7
6
5


X DAC
X AMPLITUDE
X OFFSET
X ANALOG
-5V TO 50 ohm load max
50 ohm load
U41 gain set at -1.
Y DAC
Y AMPLITUDE
Y OFFSET
Y ANALOG
U43 gain set at -1.
INTENSITY DAC
INTENSITY AMPLITUDE
INTENSITY OFFSET
IA ANALOG INTENSITY
+1V TO 50 ohm load
SYNCHRONOUS DIVIDE BY 4
INDEX "A" COUNTER
SIZE
F
CAGE CODE
55910
DRAWING NUMBER
0128490
SCALE: NONE
SHEET 7
02-01-94 14:12:00

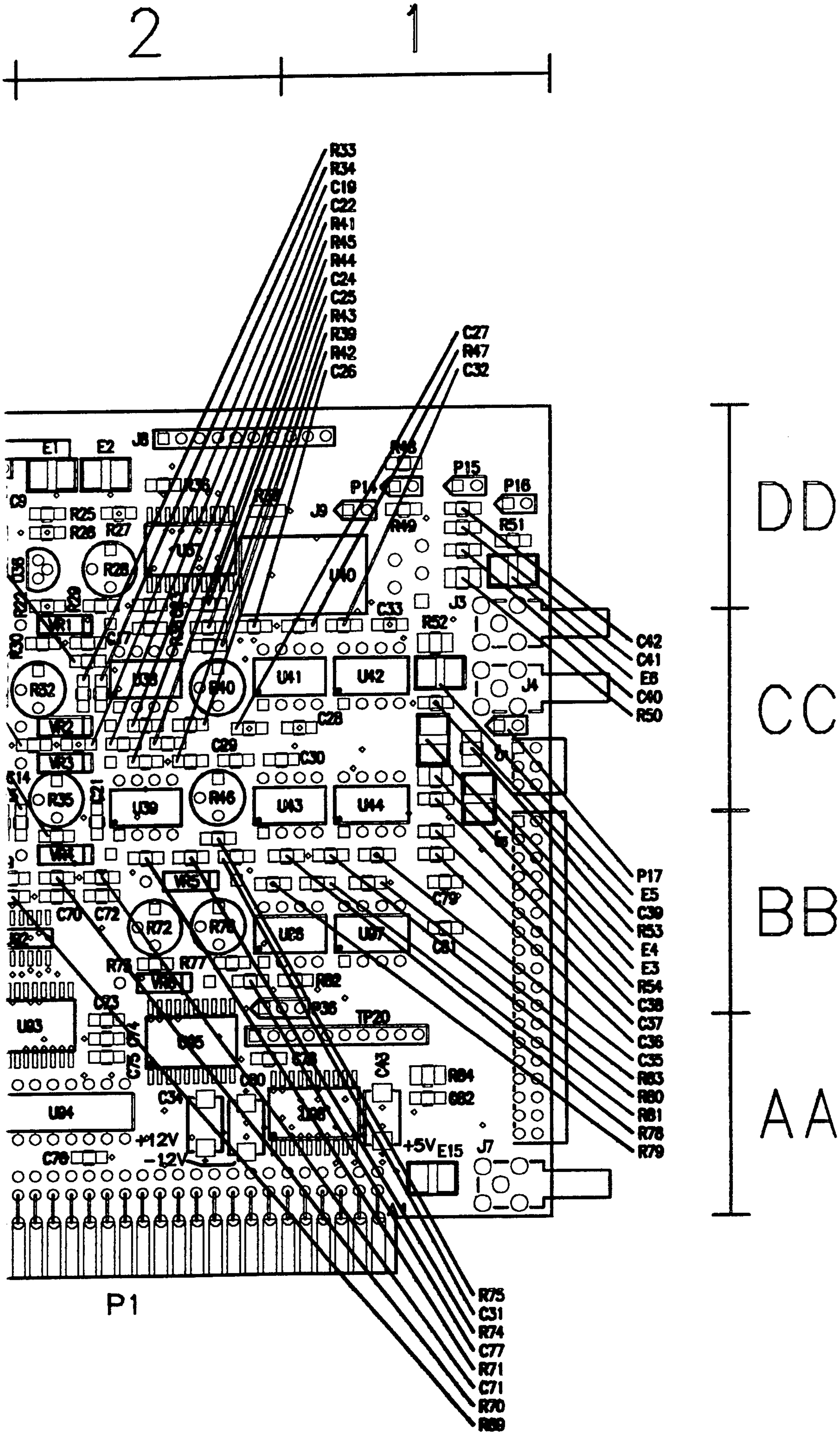


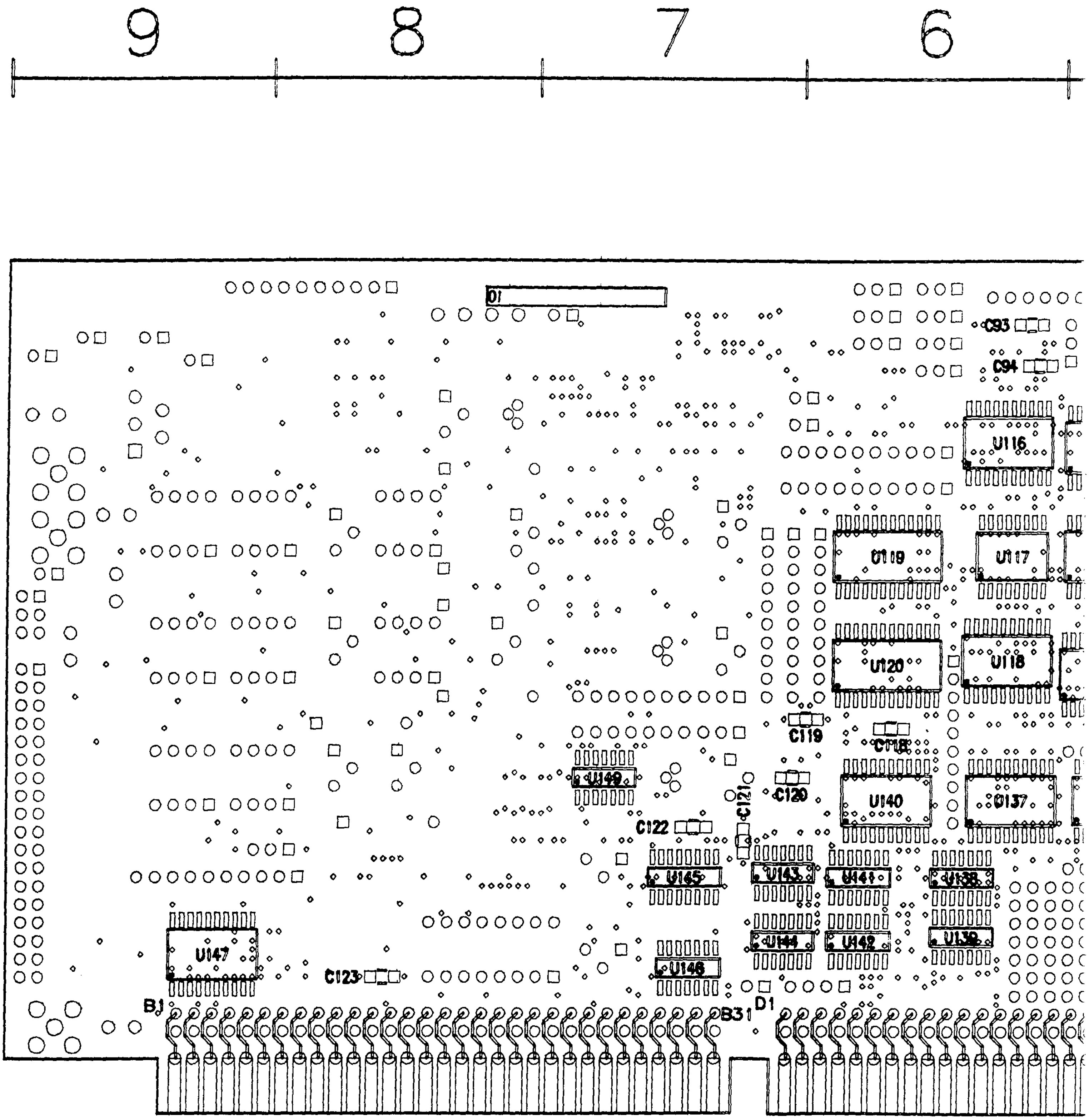
SILKSCREEN COMPONENT SIDE

LAYER 1

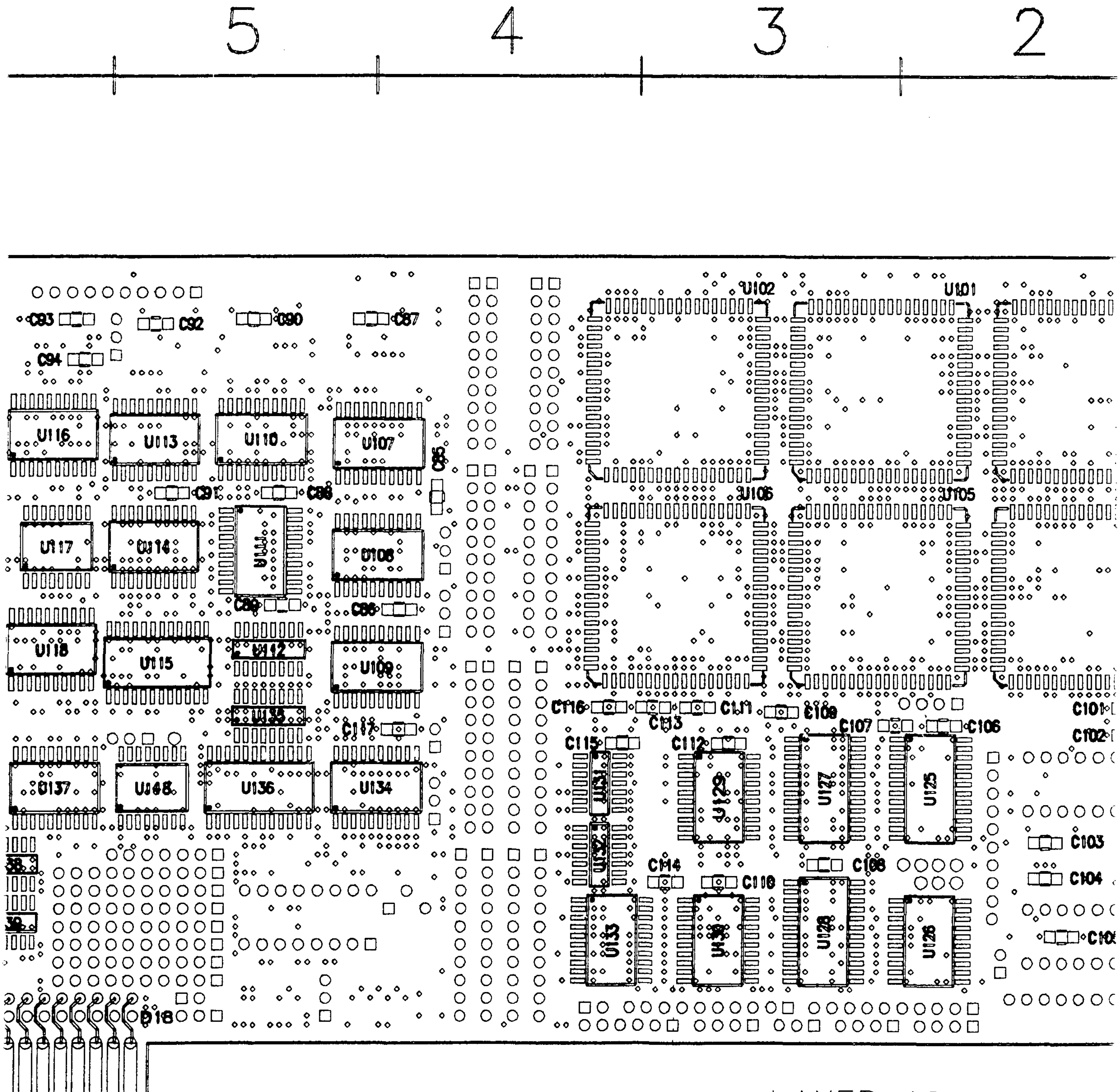

6
5
4
3
2
R31
C11
C13
C10
C18
C12
C20
R24
R10
R23
R9
R14
R18
R12
TP7
P4
P5
P6
P7
NRaD VOLUMETRIC #2 SN
P3
P32
P34
P33
P35
J10
J11
J12
TP5
Y1
+12V
C1
A31
R80
R81
TP19
TP18
TP17
TP16
TP15
P12
TP13
TP14
P2
P1

0128490 VD2


2
1
R33
R34
C19
C22
R41
R45
R44
C24
C25
R43
R39
R42
C26
C27
R47
C32
C42
C41
E6
C40
R50
P17
E5
C39
R53
E4
E3
R54
C38
C37
C36
C35
R83
R80
R81
R78
R79
R75
C31
R74
C77
R71
C71
R70
R69
DD
CC
BB
AA
P1
+12V
-12V
+5V
E15
J7
J3
J4
J8
J9
P14
P15
P16
TP20
U41
U42
U43
U44
U39
U40
U83
U84
U85
E1
E2



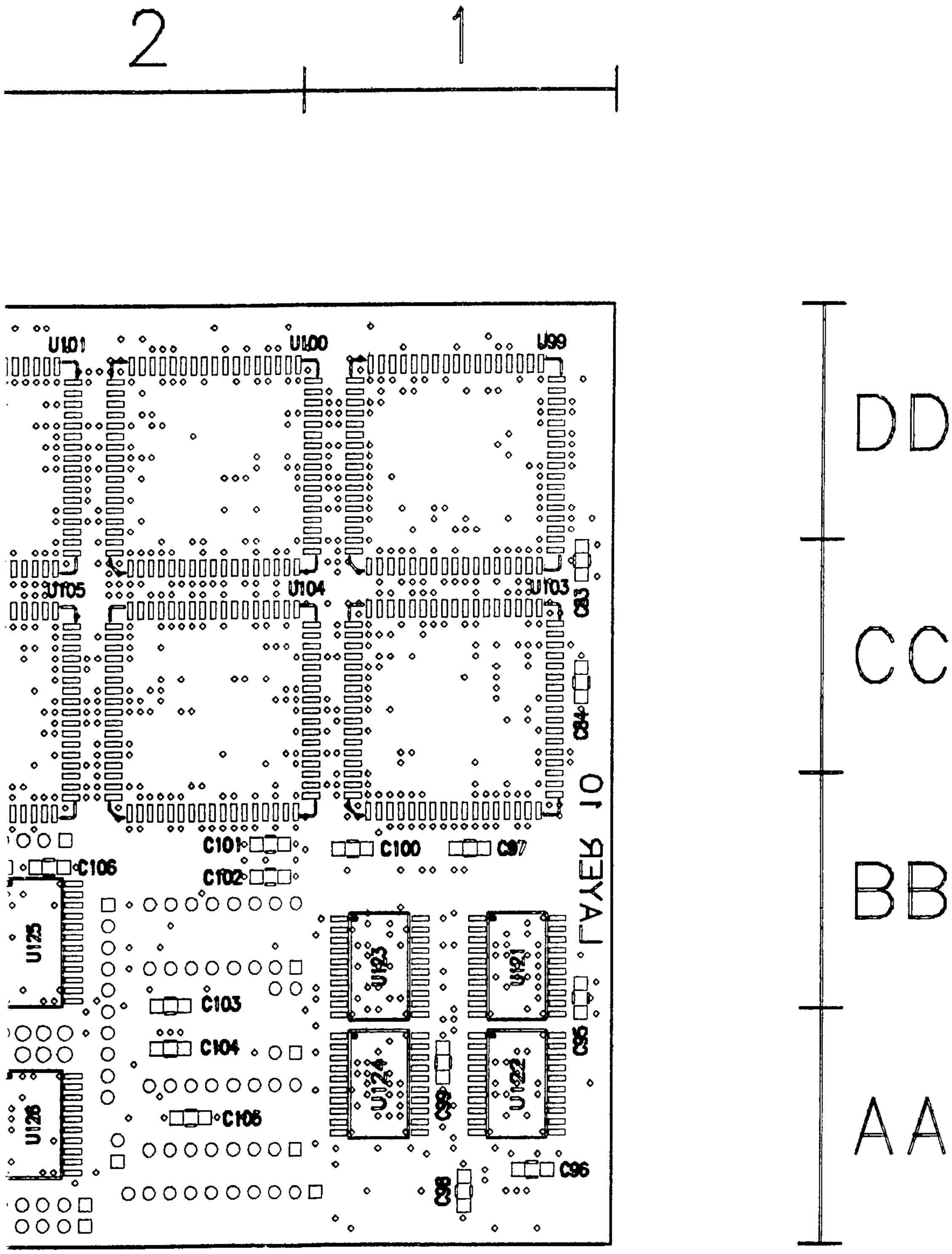
9
8
7
6
D1
C93
C94
U116
U119
U117
U120
U118
C119
C118
U149
C120
C121
U140
U137
C122
U145
U143
U141
U138
U147
U144
U142
U139
U146
C123
B1
B31
D1



LAYER 10

SIDE

0128490 VD2



10 SILKSCREEN SOLDER SIDE 01

SECTION 4. 3-D SOFTWARE

Neil Acantilado, 3-D System Software Lead Engineer.

SECTION 4
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Figures

SECTION 4. 3-D SOFTWARE

1. BACKGROUND

The Space and Naval Warfare Systems Center, San Diego, Code D44215, is developing a unique 3-D Volumetric Display System capable of displaying 3-D laser-generated images in a true 3-D spatial volume chamber. Unlike current "state-of-the-art" 3-D technologies, the 3-D Volumetric Display allows for natural physiological depth cues to occur upon viewing: motion parallax, accommodation, and binocular disparity.

The 3-D Volumetric Display System incorporates a spinning helical surface to generate a 3-D volumetric imaging chamber. To maintain an adequate image refresh rate of 20Hz, the helical surface is rotated at approximately 600 rpm. Laser light beams can then be projected into the imaging chamber through use of acousto-optic (AO) laser scanners that are controlled by onboard electronics embedded within an IBM-compatible PC. This process produces illuminated volume points (voxels) within the display chamber. The control and synchronization of the PC, the AO scanners, and the rotating helical surface is handled via specialized SSC San Diego-designed electronic control cards.

To the observer, each illuminated voxel appears to emanate from a point that has an x–z coordinate determined by the scanned laser beam and a y-coordinate determined by the height of the helix at the moment it is illuminated.

Ultimately, the overall goal of the 3-D Volumetric Display is to provide both the scientific and commercial community with a high-resolution multi-colored 3-D display system that is capable of real-time presentations of 3-D images.

2. INTRODUCTION

Software is an important and integral design component of the 3-D Volumetric Display System. It is largely responsible for the provision of essential services for daily system operation: 3-D image rendering, system maintenance and trouble–shooting, and 3-D application presentations. Furthermore, software can provide developmental tools that will aid in the development and implementation of specialized 3-D applications (i.e., air traffic control, LINK-16, and an anti-submarine warfare scenario).

This technical document will hopefully give the reader the basic knowledge and understanding of how to use the current implementation of the 3-D Volumetric Display software. It should also provide many programming tips with which an application programmer can implement his/her own version of software.

Even though some basic concepts of programming the 3-D Volumetric Control Cards are explained, it is highly recommended for the programmer to have a firm general understanding of the 3-D Volumetric #2 Control Cards before reading this section. Please refer to Section 3 of this report for more information.

3. GENERAL SOFTWARE DESCRIPTION AND SPECIFIC IMPLEMENTATIONS

The 3-D Volumetric Display Software was originally implemented on a DOS-based 486DX2 50 MHz PC with 8 MB RAM. It was coded using the Zortech C/C++ compiler (v3.1) in conjunction with the FlashTek X–32VM DOS Extender. The X–32VM DOS Extender was necessary to allow the software to have 32-bit memory addressibility to the 3-D Volumetric Control Card RAM.

A PENTIUM 166 MHz, 32 MB RAM machine replaced the 486 machine and the appropriate software modifications were incorporated to take advantage of the later machine.

NOTE: All examples of sample code provided in this section and throughout the document have been implemented using the Zortech C/C++ (v3.1) compiler. It is not guaranteed to execute under other compilers.

3.1. HIGH-LEVEL OBJECT-ORIENTED CLASSES

Since the 3-D Volumetric Display software uses an Object-Oriented design to facilitate development of specialized 3-D applications, basic C++ Object classes were implemented to furnish a core developmental software engine for the programmer. The C++ Object classes are described in in the following paragraphs.

The VCC Class instantiates a high-level software control interface that takes care of all the necessary low-level protocols involved with communicating with the 3-D Volumetric Electronic Control Cards. The VCC Class is largely responsible for the actual rendering of voxels in the display volume. Refer to the source files VCC.CPP and VCC.HPP for actual implementation.

The MATRIX Class provides the mathematical routines needed to provide appropriate coordinate matrix operations. Transformations, translations, and orientations can be performed using this class. Refer to the source files MATRIX.CPP and MATRIX.HPP for actual implementation.

The POINT Class instantiates objects that store three floating-point values. These values may be used to indicate a 3-D point in space, or it may represent a desired orientation, in which case, the values can represent the desired angles to rotate the X-, Y-, and Z-axis. Refer to the source files POINT.CPP and POINT.HPP for actual implementation.

The LINE Class allows for the rendering of 3-D lines within the display volume. A self-contained 3-D line rendering algorithm is housed within this class. Line resolution, orientations, and axis scale definitions can be user-specified if desired. Refer to the source files LINE.CPP and LINE.HPP for actual implementation.

The TEXT Class provides the capability to generate scaleable text strings within the display volume. The individual text characters are obtained from character bitmaps that are hard-coded within the class. If more desirable, vector character fonts are also provided. Refer to source files TEXT.CPP and TEXT.HPP for actual implementation.

As stated before, the intended purpose of the above classes is to provide a core developmental engine for a programmer to create meaningful 3-D applications. It is by no means the only set of classes that are used, but they probably would be essential to start. Other classes my be implemented to fulfill the specific needs of an applications.

As an example, a CONE Class was created for the 3-D demo application known as the "Cone-of-Approach" scenario. The CONE Class instantiates objects that allow for the rendering of a cone shape within the display volume. Another example is the CURSOR Class that was implemented to act as a 3-D cursor for the air traffic control application.

3.2. LOW-LEVEL I/O FUNCTIONS (VCC CLASS MEMBER FUNCTIONS)

This section will describe the actual VCC Class member functions used to communicate with the 3-D Volumetric Control Cards via the Volumetric #2 I/O Command Set. Most of the member functions utilize the INP, INPW, OUTP, and OUTPW functions to carry out their assigned I/O command task.

set_baseIO, get_baseIO. These functions configure the starting I/O base address for the 8-bit/16-bit command set. The base IO address must correspond to the I/O address DIP switch settings on the Volumetric Control Card.

allocate_vcc_ram. Utilizing a primitive memory allocation function provided by the FlashTek DOS Extender, this function allocates a 32-bit pointer that is mapped to the appropriate physical space of the 3-D Volumetric Control Card's onboard RAM. This provides the programmer access to the on-board RAM.

set_baseAddr, get_baseAddr. Used in conjunction with allocate_vcc_ram, these functions configure the Volumetric Control Card's base RAM address. The configured base RAM address must correspond to the base RAM address DIP switch settings on the Volumetric Control Card.

set_ctr0, get_ctr0. These functions program the Timer 0 clock of the 82C54–2 timer chip on-board the Volumetric Control Card. The value loaded in the Timer 0 clock corresponds to the on-time of an individual voxel. The 82C54–2 Timer chip utilizes a 10 MHz clock.

set_initreg, get_initreg. These functions configure the initial register of the Volumetric Control Card. The value loaded in the initial register will determine the starting page location in RAM for each display refresh.

set_maxvoxels, get_maxvoxels. These functions will configure the maximum number of voxels per display page.

get_shaftcount. This function will read the shaft count register. The value in the shaft count register is the number of 156.25 KHz cycles per single-helix revolution. This value will be continuously updated at every 0-degree pulse obtained from the rotating helical surface. This function is useful for speed calibration.

set_motorsetting, get_motorsetting. These functions will configure the speed of the rotating helical surface. A value ranging from 0 to 0xFFFF can be used as the motor-setting input.

set_parreg, get_parreg. These functions will configure the parameter based on a 16-bit input word. The parameter register is responsible for enabling/disabling specific functionality and states of the Volumetric Control Card. The functionality bitmap for the 16-bit word is as follows:

- Bit position 0 enables/disables the Timer 0 clock of the 82C54–2 timer chip.
- Bit position 1 enables/disables the Timer 2 clock of the 82C54–2 timer chip.

- Bit position 2 defines whether current board is a Master or a Slave.
- Bit position 3 defines whether a computer IRQ 10 is to be utilized for the system 0 pulse index.
- Bit position 4 defines whether a computer IRQ 11 is to be utilized for the system 180 pulse index.
- Bit position 5 defines whether a computer IRQ 15 is to be utilized for the paging mechanism.

Not all of the I/O commands on the Volumetric Control Card are utilized in the VCC Class. For a complete description of the Volumetric #2 Command Set, refer to Section 3 of this report.

NOTE FOR THE NOVICE PROGRAMMER: To issue commands to the 3-D Volumetric Display Control Cards, low-level I/O calls are used (INP, INPW, OUTP, OUTPW). In the case that it is not initially obvious to the programmer of how to issue Volumetric #2 commands to the 3-D Volumetric Control Cards, the following templates can be used, if desired.

If issuing an 8-bit read command to the 3-D Volumetric Control Card, the following template can be used:

```
return_value = INP(base_IO + command),
```

where return_value is the value returned from the read I/O call, base_IO is the I/O base address of the control card, and command is a defined command from the command set.

If issuing an 8-bit write command to the 3-D Volumetric Control Card, the following template can be used:

```
OUTP(base_IO + command, input_value),
```

where input_value is an 8-bit value.

The above templates also apply for the 16-bit Volumetric #2 commands, except that the INPW and OUTPW function calls are used.

3.3. CONFIGURING BASE MEMORY AND I/O ADDRESSES FOR 3-D VOLUMETRIC DISPLAY

To avoid system resource conflicts, both the Base Memory Address and the Base I/O Address are reconfigurable via DIP switches on the second-generation 3-D Volumetric Control Cards. DIP Switches #1 and #2 configure the Base I/O Address, and DIP Switch #3 configures the Base Memory Address.

3.3.1. DIP Switch Setting Examples

The current Base I/O Address of the 3-D Volumetric Control Card designated for the green-laser scanner is configured as 0240 (hex). Thus, all the switches on DIP Switch #1 should be set to ON, except for the seventh switch (which should be set to OFF). For DIP Switch #2, its first switch should be set to ON and the second switch should be set to OFF.

Memory Base I/O Address in hexadecimal: 0240

Memory Base I/O Address in binary: 0000 0010 01

DIP Switch #1 Setting: ON ON ON ON ON ON OFF ON

DIP Switch #2 Setting: ON OFF

The current Base Memory Address of the 3-D Volumetric Control Card designated for the green-laser scanner is configured as F00000 (hex). Thus, the first four ON/OFF switches of DIP Switch #3 should be set to OFF and the remaining switches should be set to ON.

Base Memory Address in hexadecimal: F 0 0 0 0 0

Base Memory Address in binary: 1111 0000 0000 0000 0000 0000

DIP Switch #3 Setting: OFF OFF OFF OFF ON ON ON ON ON ON ON ON ON ON ON ON

ON ON ON ON

Note the correspondence between the binary representations of the addresses and the DIP Switch settings.

3.4. PROGRAMMING TIMER 0 CLOCK OF 82C54–2 TIMER CHIP

Since setting the Timer 0 clock is a very essential operation, the sample code below illustrates how the VCC member function, set_ctr0, is implemented. Basically, the programming of the 82C54–2 Timer chip involves three low-level I/O function calls. The first I/O call will configure the 82C54–2 chip into the appropriate functional mode. To ensure proper hardware functioning, the Timer 0 clock must be in a "divide-by-N" mode, or Mode 2. The second and third call input the actual Timer value into the chip. More specifically, the second function call will load the lower 8 bits of the desired Timer value and the third function call will load the higher 8 bits.

```
//
// DEFINE statements
//
#define MODE2 0x4               // MODE2 will configure the 82C54-2 chip
                                // into adivide-by-N mode, as required by
                                // the 3-D Volumetric System hardware
#define RWBOTH 0x30             // RWBOTH will allow the reading and
                                // writing of the chip.
#define CTR0 0x0                // CTR0 identifies that the Timer 0 clock
                                // is to be used.
//
// 8-BIT I/O commands
//
#define cmdCtrCsCw 0x23         // 8-bit command for the 82C54-2
                                // control word.
#define cmdCtr0Cs 0x20          // 8-bit command for the 82C54-2
                                // Timer 0 clock.
```

```
#define cmdSelCtrBCtUp 0x25 // 8-bit command to configure the
                            // clock to count
                            // incrementally.

//
// GLOBAL variables
//
unsigned base_IO;           // Will contain the base I/O address for
                            // current card. Should be initialized upon
                            // VCC instantiation.

//
// VCC::set_ctr0
//
void VCC::set_ctr0(unsigned value)
{
   outp(base_IO + cmdCtrCsCw, MODE2 | RWBOTH | CTR0);  // Configure the
                                                       // the 82C54-2
                                                       // chip.
   outp(base_IO + cmdCtr0Cs, 0x00FF & value);          // Load lower
                                                       // eight bits of
                                                       // input value.
   outp(base_IO + cmdCtr0Cs, value >> 8);              // Load upper
                                                       // eight bits of
                                                       // input value.
 }
```

3.5. 3-D VOLUMETRIC RAM MEMORY ACCESSIBILITY

3-D Volumetric RAM accessibility is handled by specialized member functions of the VCC Class. Recall that almost all of the low-level communications with the 3-D Volumetric Control Cards are handled by member functions defined in the VCC Class. However, it would be very beneficial and insightful for the application programmer to study how memory addressibility is actually accomplished and implemented in the software.

The 3-D Volumetric Control Card RAM has a capacity of 65,536 32-bit words, where each memory cell word is defined to store a 12-bit X-deflection value, a 12-bit Y-deflection value, and an 8-bit intensity value. The mentioned 32-bit word is used to represent a voxel after it has been transformed from a 3-D point, a process that will be explained later in the document.

Unfortunately, access to the 3-D Volumetric RAM is not easily implementable without using additional development utilities. Since the 3-D Volumetric Control Card RAM can have a memory base address above 1 MB, a third-party DOS Extender, namely the FlashTek X–32VM DOS Extender, had to be utilized (in conjunction with the Zortech C++ compiler) to provide high-memory access for the programmer. A simple sample program for memory access is given below.

Sample code for 3-D Volumetric Display Memory Access (Example #1):

```
//
// INCLUDE STATEMENTS
//
#include <x32.h>
//
// DEFINE statements
//
#define MEM_BASE_ADDR 0xF00000
#define BYTE_SIZE 262144
#define NUM_MEM_CELLS 0xFFFF
//
// MAIN
//
void main (void)
{
  unsigned *mem_ptr = NULL;
  mem_ptr = (unsigned *) _x32_map_physical_memory(MEM_BASE_ADDR, BYTE_SIZE);
  // Load values into Volumetric RAM
  for (unsigned i = 0; i < NUM_MEM_CELLS; I++)
  {
    mem_ptr[i] = i;
  }
  // Read and print values from Volumetric RAM
  for (i = 0; i < NUM_MEM_CELLS; I++)
  {
    printf("Memory cell [%d] contents = %x\n", i, mem_ptr[i]);
  }
}
```

In most cases (almost all, in fact), it is highly desirable for a programmer to individually control and initialize the memory cell components (X-deflection, Y-deflection, and Intensity). The below sample program illustrates how this can be done.

Sample code for 3-D Volumetric Display Memory Access(Example #2):

```
//
// INCLUDE STATEMENTS
//
```

```
#include <x32.h>
//
// DEFINE statements
//
#define MEM_BASE_ADDR 0xF00000
#define BYTE_SIZE 262144
#define NUM_MEM_CELLS 0xFFFF
//
// TYPEDEF, STRUCT statements
//
typedef union voxel_struct
{
  unsigned voxel;
  struct
  {
    i: 8;
    y: 12;
    x: 12;
  } vox;
} VOXEL_STRUCT;
void main (void)
{
  VOXEL_STRUCT voxel;
  unsigned *mem_ptr = NULL;
  unsigned input_value = 0;
  mem_ptr = (unsigned *) _x32_map_physical_memory(MEM_BASE_ADDR, BYTE_SIZE);
  // Load voxels into Volumetric RAM
  for (unsigned i = 0; i < NUM_MEM_CELLS; I++)
  {
        input_value = i % 4096;
      voxel.vox.x = input_value;
      voxel.vox.y = 4095 – input_value;
      voxel.vox.i = i % 15;
      mem_ptr[i] = (unsigned) voxel.voxel;
  }
```

```
    // Read and print values from Volumetric RAM
    for (i = 0; i < NUM_MEM_CELLS; I++)
    {
        voxel.voxel = (unsigned) mem_ptr[i]);
        printf("Memory cell [%d] contents = %x, ", i, voxel.voxel);
        printf("where X = %x, Y = %x, and I = %x\n", voxel.vox.x, voxel.vox.y, voxel.vox.i);
    }
}
```

3.6. IMPORTANT "HOLE-IN-MEMORY" ISSUE

During system development and integration, major memory problems arose when the 3-D Volumetric Control Cards were installed in PCs with 16 MB RAM. During troubleshooting, the addressibility range of the 3-D Volumetric Display memory overlapped with the addressibility range of the computer RAM, thus causing memory conficts.

As a result, attempts to directly access Volumetric Display memory resulted in the direct access of computer memory. One viable solution to remedy the memory overlap was to downgrade the size of computer memory. However, this proved to be an undesirable resolution.

Fortunately, there are current PCs available with CMOS/BIOS setup utilities that allow for the configuration of a 1MB "hole" in computer memory setup at the 15 MB to 16 MB range. When enabled, computer memory between the 15 MB and 16 MB area will essentially be turned off and memory access within this region will be redirected to the PC ISA bus to the 3-D Volumetric Control Cards. Thus, by configuring the base address of 3-D Volumetric Display memory so that it falls within this 15 MB to 16 MB area, memory conflicts will no longer be a problem.

The CMOS/BIOS setup utility by Award Software has this "hole-in-memory" capability.

3.7. 3-D VOLUMETRIC INTERRUPT HANDLING

As indicated in the description of the parameter register word, the 3-D Volumetric Control Cards are able to send IRQ interrupt requests to the computer in response to a particular trigger event, where they can be serviced by a corresponding Interrupt Service Routine (ISR). It is left to the programmer to provide the necessary instructions to be carried out for the ISR.

Specifically, an IRQ10 interrupt request is sent to the computer whenever a 0-degree system index pulse is received from the helix sensor mechanism. Similarly, an IRQ11 interrupt request is sent to the computer whenever a 180-degree system index pulse occurs. An IRQ15 interrupt request is sent to the computer whenever a configured page of voxels has been refreshed.

IMPORTANT: In addition to servicing and adequately handling volumetric IRQ interrupt requests on the computer side, it is also the responsibility of the programmer to clear those same IRQ request lines on the 3-D Volumetric Control Card. This is done through use of the appropriate interrupt clear I/O functions made available in the Volumetric #2 command set.

3.8. SAMPLE CODE FOR INTERRUPT HANDLING

When executed, the below sample program will set up an Interrupt Service Routine for IRQ 10 that will count the number of 0-degree system index pulses obtained from the helix sensors.

```
//
// DEFINE statements
//
#define INTCTR1 0x20
#define INTCTR2 0xA0
#define IRQ10_VECT 0x72
#define IRQ11_VECT 0x73
#define IRQ15_VECT 0x77
#define NSEOI 0x20
#define EN_IRQ10 ~(1 << 2)
#define EN_IRQ11 ~(1 << 3)
#define EN_IRQ15 ~(1 << 6)
//
// GLOBAL variables
//
unsigned baseIO = 0x240
unsigned volatile count = 0;
unsigned int_config;
//
// IRQ10_ISR (Interrupt Service Routine for IRQ10)
//
static int _cdecl IRQ10_ISR(INT_DATA *pd)
{
  count++;
  inp(baseIO + 0x21);
  outp(INTCTR1, NSEOI);
  outp(INTCTR2, NSEOI);
  return 1;
}
//
// MAIN
//
void main(void)
```

```
{
  set_ctr0(18);
  set_parreg(0xFF);
  set_motorsetting(3180);
  init_intercept(IRQ10_VECT, IRQ10_ISR, 0);     // Set ISR for IRQ10
  int_config = inp(INTCTR2 + 1);                // Get current Int Controller config
  outp(INTCTL2 + 1, int_config & EN_IRQ10);     // Activate IRQ10

  while (!kbhit())
  {
    printf("%d\n", count);
  }
  outp(INTCLT2 + 1, interrupt_config);     // Restore original Int Ctr config
  int_restore(IRQ10);                      // Restore original ISR for IRQ10
}
```

4. 3-D VOXEL RENDERING

Since the voxel-rendering algorithm defined in the VCC Class is a very necessary and essential service of the 3-D Volumetric Display Software, this section presents a general synopsis of the involved process.

4.1. BACKGROUND AND ISSUES

On the 3-D Volumetric Control Cards, there exists a dual-port memory RAM that is responsible for the storage of image display voxels. An X-deflection value, a Y-deflection value, and an intensity value define the specific content of each RAM memory cell.

To produce an image, each RAM memory cell is sequentially traversed for its "voxel" content (x-defl, y-defl, intensity), where it is then fed directly to the acousto-optic laser scanner. The speed at which RAM is traversed depends upon the Timer 0 clock value configuration. (For example, a Timer 0 clock value of 13 will configure a memory cell readout rate of 1300 nanoseconds, or 1.3 microseconds). The X–Y deflection values are used by the laser scanner to deflect the outgoing laser beam accordingly. The voxel intensity value is used by the laser modulator mechanism to control the brightness of the deflected beam. The X–Y deflection values range from 0 to 4095 and the intensity value can range from 0 to 255.

In essence, a memory cell in the dual-port memory RAM represents a specific "snapshot" rotation position of the spinning helical surface. Hence, a correspondence between memory cells and the height of the helical surface can be achieved as a function of time (which in turn is dependent upon the Timer 0 clock).

Thus, the major tasks in voxel-rendering becomes 1) the mapping of the X–Y coordinate values of the 3-D voxel to corresponding low-level laser scanner deflection values and, 2) the identifying of the specific timeslice memory cell to be derived from the Z coordinate value.

4.2. 3-D VOLUMETRIC DISPLAY COORDINATE SYSTEMS

All 3-D images to be processed and rendered will be transformed from the World Coordinate System to the Helix Coordinate System to the (Quadrant) Scanner Coordinate System.

The World Coordinate System is defined as a general 3-D coordinate system. In other words, it is a coordinate system that is not restricted with boundaries.

The Helix Coordinate System is a 3-D coordinate system normalized to the actual physical dimensions of the display volume, where its origin exists in the center of the helix. For example, if the diameter of the helix is 36-inches and the height of the helix is 18-inches, then $\{-18 \le X \le 18, -18 \le Y \le 18, 0 \le Z \le 18\}$ are the boundaries of this coordinate system.

Finally, the Scanner Coordinate System is defined as a 2-D System that is mapped to the range of deflection values of the laser scanners, which are defined as $\{0 \le \text{x–defl} \le 4095, 0 \le \text{y–defl} \le 4095\}$. Since four laser scanners are used in a four-quadrant imaging region (per color), four different quadrant transformations must be defined.

4.3. A QUADRANT TRANSFORMATION EXAMPLE

PROBLEM

Given the information below, derive the appropriate linear transformation equations for each helix quadrant. (Refer to figure 4-1).

Suppose we have a Helix Coordinate System as described in the above section, where $\{-18 \le x \le 18, -18 \le y \le 18, 0 \le z \le 18\}$.

Define Quadrant A as being located in the upper left quadrant of the Helix Coordinate System, where the Helix coordinates along $\{-18 \le x \le 0, 0 \le y \le 18\}$ directly correspond (as a one-to-one mapping) to the Scanner coordinates along $\{0 \le \text{x–defl} \le 4095, 0 \le \text{y–defl} \le 4095\}$.

Define Quadrant B as being located in the upper right quadrant of the Helix Coordinate System, where the Helix coordinates along $\{-18 \le x \le 0, -18 \le y \le 0\}$ directly correspond (as a one-to-one mapping) to the Scanner coordinates along $\{0 \ge \text{x–defl} \ge 4095, 0 \ge \text{y–defl} \ge 4095\}$.

Define Quadrant C as being located in the lower left quadrant of the Helix Coordinate System, where the Helix coordinates along $\{0 \le x \le 18, -18 \ge y \ge 0\}$ directly correspond (as a one-to-one mapping) to the Scanner coordinates along $\{0 \le \text{x–defl} \le 4095, 0 \ge \text{y–defl} \ge 4095\}$.

Define Quadrant D as being located in the lower right quadrant of the Helix Coordinate System, where the Helix coordinates along $\{0 \le x \le 18, 0 \le y \le 18\}$ directly correspond (as a one-to-one mapping) to the Scanner coordinates along $\{0 \le \text{x–defl} \le 4095, 0 \le \text{y–defl} \le 4095\}$.

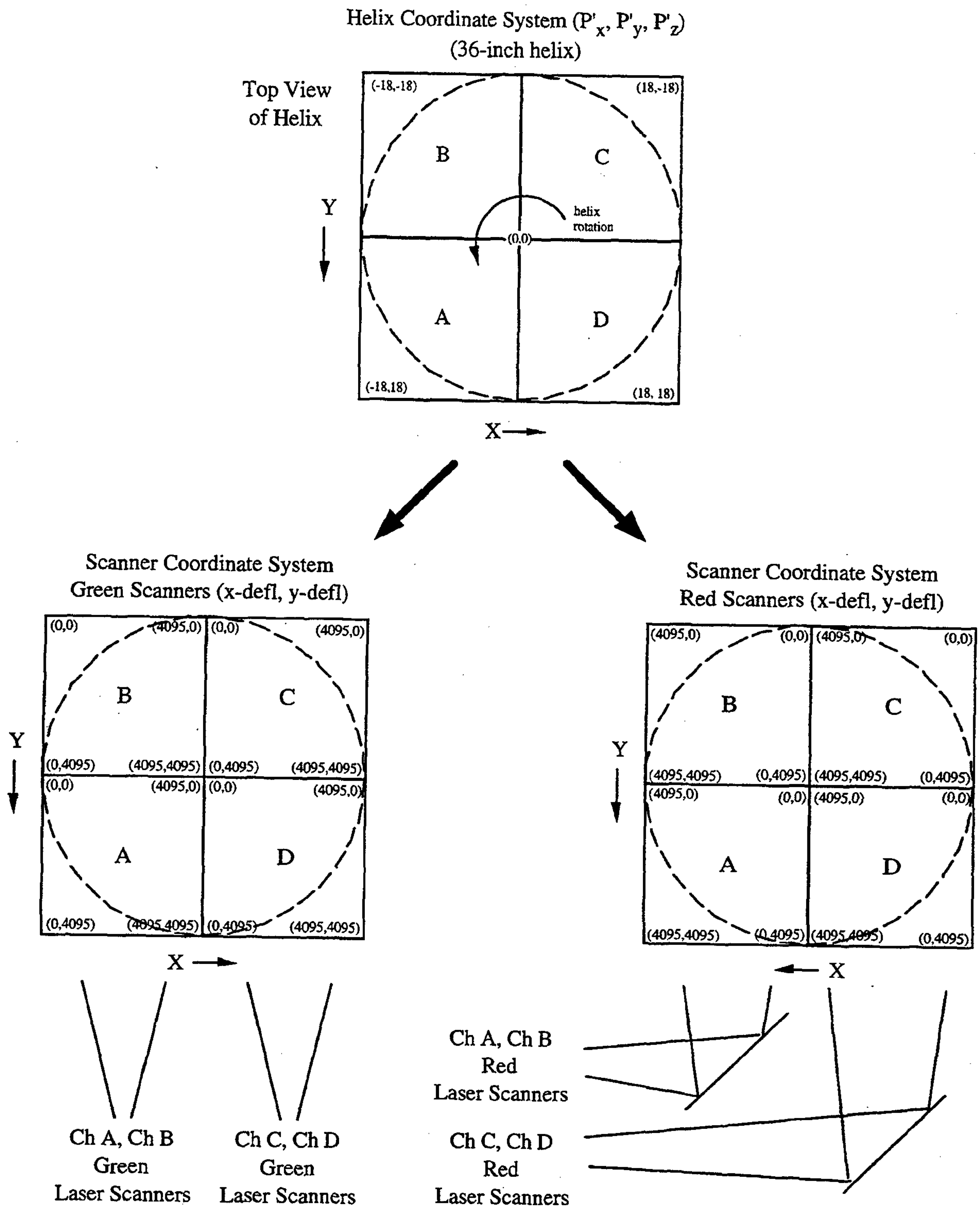

Figure 4-1. Helix four-quadrant transformations for green and red scanners (36-inch system).

SOLUTION

Denote P' as a 3-D point in the Helix Coordinate System, where P'x, P'y, and P'z are its coordinate components.

Green Scanner Transformations

If P' resides in Quadrant A, then:

x–defl = (P'x + 18) x 4095/18

y–defl = (P'y – 0) x 4095/18

If P' resides in Quadrant B, then:

x–defl = (P'x + 18) x 4095/18

y–defl = (P'y + 18) x 4095/18

If P' resides in Quadrant C, then:

x–defl = (P'x – 0) x 4095/18

y–defl = (P'y + 18) x 4095/18

If P' resides in Quadrant D, then:

x–defl = (P'x – 0) x 4095/18

y–defl = (P'y – 0) x 4095/18

Red Scanner Transformations

If P' resides in Quadrant A, then:

x–defl = – (P'x – 0) x 4095/18

y–defl = (P'y – 0) x 4095/18

If P' resides in Quadrant B, then:

x–defl = – (P'x – 0) x 4095/18

y–defl = (P'y + 18) x 4095/18

If P' resides in Quadrant C, then:

x–defl = – (P'x – 18) x 4095/18

y–defl = (P'y + 18) x 4095/18

If P' resides in Quadrant D, then:

x–defl = – (P'x – 18) x 4095/18

y–defl = (P'y – 0) x 4095/18

4.4. 3-D VOLUMETRIC DISPLAY MEMORY

As stated earlier, the 3-D Volumetric Display Memory is essentially a list that stores voxel data for an image or scene to be displayed, where each memory cell entry (whether empty, or not) is individually traversed and read out to the laser scanner sequentially. The scanner uses the information contained in the traversed entry to produce a deflected beam of laser light within the display chamber. There is a maximum of 65,535 memory cell entries in the 3-D Volumetric Display memory.

Since list traversal is synchronized with helix rotation, the location of a memory cell correlates to a specific angular orientation of the helical surface. It is the orientation position of the helical surface at the exact memory cell read-out time that provides the height for a particular voxel entry. Traversal restarts at the beginning of the voxel list when the leading edge of the rotating helical surface trips the 0-degree (or 180-degree, if available) helix sensor.

The Timer 0 clock determines the read-out rate of each memory cell and it can be configured to suit the needs of the application. If desired, more voxel memory cells can be made readily available per image refresh by configuring a faster Timer 0 clock. However, there is a trade-off. The faster the Timer 0 clock, the quicker the read-out time per memory cell becomes, thus affecting the voxel on-time in the display chamber.

The location of a memory cell also determines what quadrant laser scanner to use for rendering. Assuming that display memory starts at memory cell 0 per refresh, the memory designations for each quadrant laser scanner are as follows:

All voxels stored in memory cell (N% 4) are handled by Scanner A,

All voxels stored in memory cell ((N + 1) % 4) are handled by Scanner B,

All voxels stored in memory cell ((N + 2) % 4) are handled by Scanner C,

All voxels stored in memory cell ((N + 3) % 4) are handled by Scanner D,

where N represents a cell number ranging from 0 to 65,535 and % is the binary MODULO integer operation.

4.5. DETERMINATION OF TIMER 0

At a minimum, a 20-Hz refresh rate is highly desirable for the 3-D Volumetric Display System. Any rate less than 20 Hz will cause the image, or scene within the display chamber to flicker. To maintain a 20-Hz refresh rate, the Timer 0 clock must be configured correctly to do so. A general equation for determining a Timer 0 clock value is

$$T0 = 10^{-7} / (R*V) ,$$

where R is the desired refresh rate and V is the maximum number of voxels configured to be refreshed in a single frame (or single helix rotation). Recall that a 10-MHz clock is being fed into Timer 0, thus a T0 value will produce a memory cell read-out at every (T0 * 100) nanoseconds. Because of the random access mode of scanning, there is a 5 μs delay, or "acoustic fill-time" between points. Taking this into consideration, as well as the four channels of the scanner, the voxel on-time can be calculated. As an example, for a T0 clock value of 13, the voxel on-time is

$$\text{Voxel On-Time} = (13 * 0.1\mu s * 4) - 5\mu s = 0.2\mu s .$$

Similarly, for a T0 clock value of 30 we have,

$$\text{Voxel On-Time} = (30 * 0.1\mu s * 4) - 5\mu s = 7.0\mu s ,$$

Thus, it can be seen that the voxel on-time increases as the clock value increases, making the image brighter at the expense of fewer voxels..

It is very important to note that the helix rotation speed must be calibrated so that the time it takes for a single rotation is synchronized exactly to the time it takes to refresh a single frame. In other words, the time it takes for one helix rotation must be equal to (T0 * 100 * V) nanoseconds.

4.6. DETERMINATION OF OPTIMAL HELIX ROTATION SPEED

The speed of the rotation of the helix is controlled by the motor control register available on the 3-D Volumetric Control Cards. Each 12-bit word loaded into the motor control register will be converted to a voltage control signal and sent to the helix motor power supply which determines the rotation speed of the helix. The 12-bit word will be converted to a voltage ranging from 0 volts to +5 volts. Use the VCC member functions set_motorsetting and get_motorsettings whenever configuring motor speed.

Also, an indication of the helix rotation speed can be obtained via use of the shaft counter read-out circuitry conveniently provided by the 3-D Volumetric Control Card. The values that are obtained from the shaft counter will denote the number of 156.25 kHz cycles counted per single helix rotation. Hence, the helix speed can be determined by the following equation:

$$\text{Helix speed} = ((156{,}250 / S) * 60) \text{ rpm},$$

where S is the shaftcount reading provided by the shaft counter circuitry. For a 600 rpm helix, S would equal 15,625 counts.

In general, if R is the required number of refreshes per second, then the helix rotation speed should reflect a shaft counter value to ensure proper synchronization with the Timer 0 clock,

$$S = (156{,}250 / R) * (\text{number of helix blades})$$

It is highly recommended to poll the shaftcount from the shaft counter should be polled so that the helix rotation speed can be monitored and regulated. Polling allows detection and correction of any speed drifts and irregularities can be readily detected and corrected before image deterioration occurs. It may be more useful to set up an Interrupt Service Routine (ISR) for IRQ10 solely dedicated for helix speed managing, where the helix speed can automatically be monitored and regulated whenever a 0-degree system index pulse occurs.

4.7. SPEED CONTROL FOR THE CURRENT 36-INCH 3-D VOLUMETRIC DISPLAY SYSTEM

This section briefly illustrates how the helix speed is handled for the current 36-inch 3-D Volumetric Display System located at Topside, Building 33, Lab 0426.

Due to the utilization of a double-helix in the 36-inch 3-D Volumetric Display System, a helix speed of 600 rpm (as opposed to 1200 rpm) is needed to keep up with a 20-Hz refresh rate. This is because the double-helix configuration issues two system index pulses (instead of one system index pulse) in a single rotation that allows for two refreshes per revolution.

Since the current system motor yields a maximum speed of 768 rpm, a value of 3199 (derived from 600 * (4095/768)) must be loaded into the motor control register to maintain the 10 Hz speed rate. Image-rendering activity does not begin until the helix is fully up to speed.

Once up to speed, the helix rotation speed is then frequently monitored for speed anomalies, where a shaftcount reading of 15,625 cycles (derived from (156,250/10)) is expected per single revolution. If the shaftcount reading starts diverging from 15,625, then the value in the motor control register is adjusted accordingly to correct the situation.

4.8. HIGH-LEVEL DESCRIPTION OF THE VOXEL-RENDERING ALGORITHM FOR FOUR-QUADRANT SYSTEM

The following is a high-level step-by-step synopsis of the algorithm employed by the 3-D Volumetric Display Software for rendering a single voxel in the display volume. The source code for the actual algorithm implementation can be found in the view2device2memory member function found in VCC.CPP.

Let P represent a given point in 3-D space, where Px, Py, and Pz denote the x, y,

and z components of P.

Let R represent a transformation matrix containing desired translations, rotations,

axis scale definitions, etc.

Let R(P) represent P after transformation R has been applied.

Let VMEM[i] denote the ith memory cell of the 3-D Volumetric Display memory.

Let VMEM[i].x, VMEM[i].y, and VMEM[i].i denote the x, y, and intensity components of the memory cell, respectively.

1. Obtain a 3-D point **P** to be rendered containing x, y, and z coordinates, where **P** is defined in the World Coordinate System.

2. Transform **P** from the World Coordinate System to the Helix Coordinate System and denote transformed voxel as **P'**. If desired, additional transformations (rotations, translations, etc.) can be applied to **P'**. **P'** will be clipped if it is outside the acceptable boundary regions of the Helix Coordinate System. The Helix Coordinate System can be described in terms of the actual size dimensions of the helical surface where the origin exists in the center of the bottom of the helix. For example, if the diameter of the helix is 36 inches and the height of the helix is 18 inches, then use the following bounds to define the Helix Coordinate System: $-18 \le x \le 18$, $-18 \le y \le 18$, $0 \le z \le 18$. Note: In some versions of the software the y-axis is used to describe the height of the helix, where y values of 0 and 18 correspond to the bottom and top of the helix, respectively:

   Define P' = R(P). Disregard P', if P' is not within acceptable boundaries of the Helix Coordinate System.

3. Calculate the rotation angle that the leading edge of the helix will have to rotate in order for it to intersect voxel **P'**. The x-coordinate and y-coordinate of **P'** will be used in this calculation:

   $\alpha = \text{atan2}(P'.x, -P'.y)$.

   If $(\alpha < 0)$ then $\alpha = \alpha + 2\pi$.

4. Let **q** denote the helix quadrant to which **P'** belongs to. Since there is a dedicated Laser Scanner for each quadrant of the helix, the information contained in **q** will let us know which laser scanner to use for the actual rendering of **P'**. The possible values for **q** are 0, 1, 2, and 3:

   A q value of 0 indicates that P' exists in the upper left helix quadrant, B.

   A q value of 1 indicates that P' exists in the upper right helix quadrant, C.

   A q value of 2 indicates that P' exists in the lower right helix quadrant, D.

   A q value of 3 indicates that P' exists in the lower left helix quadrant, A.

   if $(\alpha > 3\pi/2)$ then q = 1.

   else if $(\alpha > \pi)$ then q = 2.

   else if $(\alpha > \pi/2)$ then q = 3.

   else q = 0.

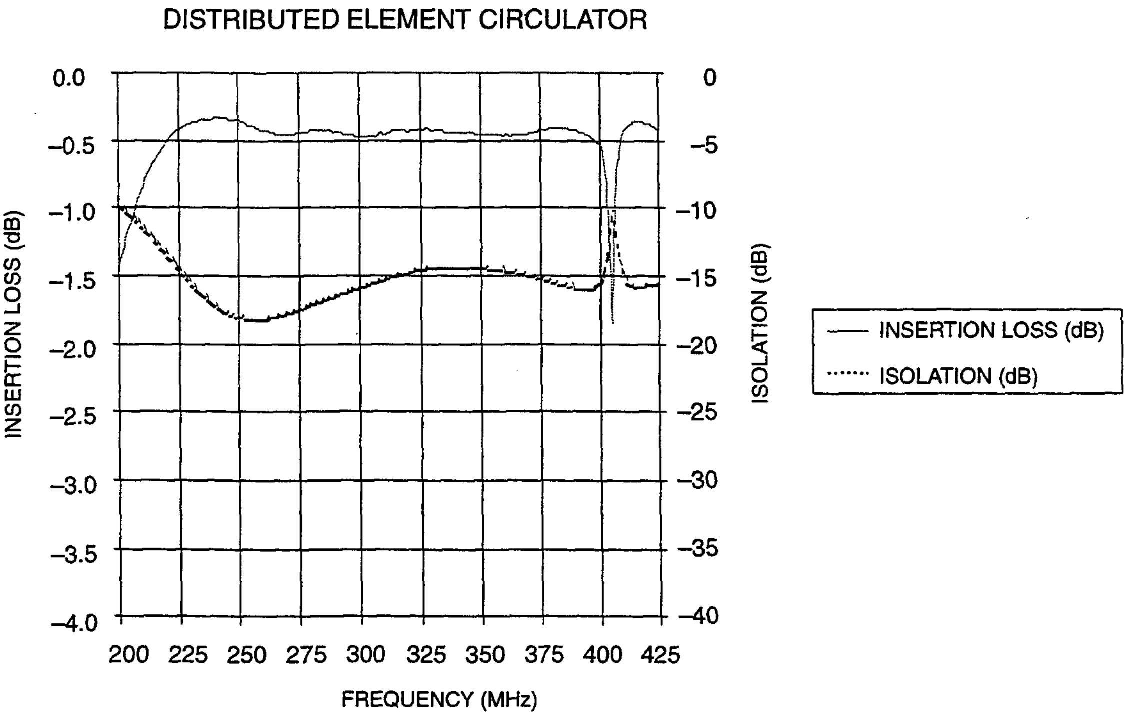

Figure 4-2. Orientation of angles used in voxel position calculations.

5. In addition to the previous rotation angle calculated, calculate the rotation angle that the leading edge of the helix will have to FURTHER rotate in order for the helix to be at the appropriate height for voxel **P'**. The z–coordinate of **P'** will be used in this calculation:

   $\beta = \beta + (P'.z / (\pi / MaxZ))$, where MaxZ is the height of the helix.

   If $(\beta > 2\pi)$ then $\beta = \beta - 2\pi$.

6. Map $\theta = \alpha + \beta$ to its corresponding memory cell in the 3-D Volumetric Display RAM. Define **i** as being the **i**th memory cell that is mapped to θ. Since the memory cell location determines the quadrant scanner to use for rendering, use the quadrant information given in **q** to adjust **i** accordingly:

   $i = (MaxVoxels / 4) * (\theta / \pi)$, where MaxVoxels is the # of voxels per refresh.

   $i = i * 4$.

   $i = i + q$.

7. Transform **P'** from the Helix Coordinate System to Scanner Coordinate System. Denote as **P''**. Defined as a 2-D coordinate system, the Scanner Coordinate System describes the actual deflection values used in the laser scanners and is bounded by the following: $0 \leq x \leq 4095$, $0 \leq y \leq 4095$. Since there are designated scanners devoted for each helix quadrant, each quadrant scanner will yield its own individual Scanner Coordinate System. Thus, using the quadrant information given in **q**, use the appropriate quadrant transformation to transform **P'** to **P''**:

   if (q == 0) then

   P''.x = (P'.x–X1_chA) * ((B4_chA–B1_chA) / (X4_chA–X1_chA)) + B1_chA.

   P''.y = (P'.y–Y3_chA) * ((A4_chA–A3_chA) / (Y4_chA–Y3_chA)) + A3_chA.

else if (q == 1) then

P".x = (P'.x–X1_chB) * ((B4_chB–B1_chB) / (X4_chB–X1_chB)) + B1_chB.

P".y = (P'.y–Y3_chB) * ((A4_chB–A3_chB) / (Y4_chB–Y3_chB)) + A3_chB.

else if (q == 2) then

P".x = (P'.x–X1_chC) * ((B4_chC–B1_chC) / (X4_chC–X1_chC)) + B1_chC.

P".y = (P'.y–Y3_chC) * ((A4_chC–A3_chC) / (Y4_chC–Y3_chC)) + A3_chC.

else

P".x = (P'.x–X1_chD) * ((B4_chD–B1_chD) / (X4_chD–X1_chD)) + B1_chD.

P".y = (P'.y–Y3_chD) * ((A4_chD–A3_chD) / (Y4_chD–Y3_chD)) + A3_chD.

8. If the **i**th memory cell is non–empty, then identify an index **j** such that **VMEM[j]** is the closest <u>empty</u> memory cell to **VMEM[i]**, and **VMEM[j]** is in the same quadrant as **VMEM[i]**. Set **i** equal to **j**.
9. Load **P"** into the **i**th memory cell:

   VMEM[i].x = P".x;

   VMEM[i].y = P".y;

   VMEM[i].i = 255;

5. 3-D VOLUMETRIC DISPLAY APPLICATIONS

This section describes some of the 3-D applications that have been implemented for the second generation 3-D Volumetric Display System. The core software engine described in section 3.1 has been used as a base building block for these 3-D applications.

5.1. ATC SPATIAL PLAN POSITION INDICATOR (SPPI) DISPLAY

The SPPI display is a 3-D version of the conventional 2-D Plan Position Indicator display used by air traffic controllers.

Like its 2-D counterpart, the SPPI display surveys target aircraft data received from a real-time IFF data feed within a 360-degree, 100-mile radius region. At every 12-second interval, detected aircraft will be appropriately updated and displayed within the display chamber. A remote-controlled 3-D cursor allows the operator to interrogate specific aircraft targets for identification and positional information. The interrogation information will be rendered in the display chamber. Also, a zoom capability is made readily available so that one can focus on an area of interest.

An important advantage of the SPPI display is its natural ability to show the attribute of altitude for aircraft.

A patent is pending for the SPPI display.

5.2. SUBMARINE UNDERSEA NAVIGATION AND ANTISUBMARINE WARFARE (ASW)

Authentic 3-D topographical undersea data obtained from a sister laboratory were successfully rendered on the 3-D Volumetric Display System. The 3-D sonar undersea data were acquired from

one of the Navy's premier underwater terrain mapping systems, the Wide Swath Array Sonar System (SASS), which uses state-of-the-art digital signal-processing technology.

As a result of a successful feasibility study, two animated hypothetical underwater scenarios using the sonar data have been generated to illustrate possible submarine usage of the 3-D Volumetric Display. The first submarine animation demonstrates an exploration scenario where a sub is navigating around an undersea mountainous region. The second animation depicts an undersea battle between two attack submarines.

5.3. 3-D ATC GLIDE SLOPE DEMONSTRATION, OR THE "CONE-OF-APPROACH"

An animated simulation was implemented to illustrate a 3-D rendition of an ATC glide-slope display. A glide-slope display, in short, helps air traffic controllers guide incoming aircraft to a landing. The current 3-D volumetric simulation utilizes a 3-D cone, referred to as the "cone-of-approach," which emanates from an optimal point on the runway and projects outward to reveal an ideal approach glide path for incoming simulated aircraft designated for landing.

The "Cone-of-Approach" demonstration scenario has been well-received by the ATC community and is being considered for future projects.

5.4. 3-D VOLUMETRIC DISPLAY INTERFACE FOR THE GENEX REAL-TIME 3-D CAMERA

As a requirement for a feasibility study, a real-time software interface scheme between the 3-D Volumetric Display and the Genex High-Speed 3-D Camera was successfully implemented.

As a result of this exciting breakthrough, BBC-TV of England has filmed and dedicated a segment on an episode of *Tomorrow's World* devoted to the 3-D Volumetric Display System.

5.5. PICTURE LIST (PL) FILE 3-D RENDERER, DXF2PL CONVERTER

Picture List (PL) files are input files containing specialized rendering information for describing a particular image to be displayed. More specifically, a PL file is an ASCII text file that will contain basic point, line, and chain declarations to define its image. The 3-D Volumetric Display Software has a built-in PL file interpreter that can read PL files and display them accordingly. Unless otherwise configured, the interpreter will automatically center the image in the display chamber, thus transforming image points and lines from World Coordinates to Helix Coordinates to Quadrant Coordinates. Refer to the function READ_PL defined in REAL_PL.CPP for actual implementation and usage.

A "DXF to PL" converter for the 3-D Volumetric Display System was implemented by NEOS Technologies, Inc. The converter will convert CAD DXF files into PL files. As it currently stands, the DXF2PL Converter is a "stand-alone" software product. Efforts are being undertaken to integrate the DXF2PL Converter functionality directly into the 3-D Volumetric Display Software.

Recently, a "Venus De Milo" DXF file was successfully ported to a PL file.

5.6. 3-D MEDICAL IMAGING

Due to the immense size of medical imagery data and the present limitations of resolution and voxel capacity, the 3-D Volumetric Display System can only render simplistic and static 3-D medical images. The current repertoire of medical images available for demonstration include the arteries of

the heart, a 3-D EKG plot, an aorta taken from MRI data, and a 3-D image of a brain-generated from 2D MRI cross-section sets.

In an attempt to be considered as a viable 3-D medical imaging display, current proposals are in the works to develop a high-resolution, multi-color 3-D Medical Volumetric Display System.

5.7. LINK-16 SOFTWARE INTERFACE FOR THE JWID 97 TRANSPORTABLE 3-D DISPLAY

In such a very short time, SSC San Diego with its industrial CRADA partners, NEOS Technologies and RGB Technologies, achieved a major milestone with the successful installation of a transportable 3-D Volumetric Display System onboard USS *John C. Stennis* at Norfolk, VA, while participating in the highly visible 1997 Joint Warrior Interoperability Demonstration.

During the month of July, situated in the Tactical Flag Command Center (TFCC) of the USS *Stennis,* the Transportable 3-D Volumetric Display System was interfaced to the Common Operational Picture (COP) data network via a live Link-16 STU–III connection to SSC San Diego.

Along with a detailed fictional JWID 97 battle scenario map, live land, air, surface, and subsurface tracks were displayed throughout the war demonstration. Like the SPPI display, track interrogation was made possible through the use of a remote trackball mouse. Also, map zooming and panning were featured and made readily available to the operator.

The transportable display was able to function without major problems even when USS *Stennis* was out to sea for 3 days.

5.8. HUMAN FACTORS 3-D STUDY

The second-generation 3-D Volumetric Display System participated in a recent human factors research study where air traffic controller subjects were required to complete specific fundamental ATC-related judgment tasks across differing 2-D/3-D display platforms. An additional Silicon Graphics Indigo 2 machine was used in conjunction with the 3-D Volumetric Display System.

The purpose of the study was to try and provide substantial data on how each display platform facilitated (or hindered) the air traffic controller with their tasks.

Subject performance data obtained from the study is currently being processed, assessed, and analyzed by the Human Factors Group.

5.9. TACTS ADDS 3-D DEMONSTRATION

Authentic flight data provided by a Miramar NAS Flight Training Facility were successfully depicted and demonstrated on the second-generation 3-D Volumetric Display System. Features of this demonstration software included flight history trails, airspace zooming capabilities, and aircraft interrogation.

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APPENDIX 4-A. THE 3-D VOLUMETRIC #2 CONTROL CARD I/O COMMAND SET

The header file V2IO.H contains the DEFINE statement declarations for the 3-D Volumetric #2 Control Card I/O Command Set. The source listing of V2IO.H will be given in this section, where a command description will be provided when necessary. Please use this section in conjunction with Section 3 of this report.

```
//*******************************************************************
//*  U.S. Government Proprietary ( 35 USC 205 )                      *
//*  This software is covered by one or more U.S. Navy owned         *
//*  patents/patent applications and/or invention disclosures.       *
//* Direct licensing inquiries to:                                   *
//*                 Harvey Fendelman                                 *
//*                 Legal Counsel for Patents                        *
//*                 NCCOSC Code D0012                                *
//*                 San Diego Ca. 92152-5765                         *
//*                 (619) 553-3001                                   *
//*******************************************************************

//
// V2IO.H
//

#ifndef V2IOH
#define V2IOH

#include <dos.h>
#include <conio.h>

//
// 16-Bit I/O Commands
//
#define cmdRdMLReg          0x00  // rd, Read ML Register
#define cmdRdXDACTbl        0x06  // rd, Read X-DAC Table
```

```
#define cmdLdXDACTbl        0x06  // wr, Load X-DAC Table

#define cmdRdYDACTbl        0x08  // rd, Read Y-DAC Table

#define cmdLdYDACTbl        0x08  // wr, Load Y-DAC Table

#define cmdRdShftRegClr     0x0A  // rd, Read Shaft Register then
                                  //  clear

#define cmdLdSpdReg         0x0A  // wr, Load Motor Speed Register

                                  // (D11 through D0)

#define cmdRdLUTInc         0x0C  // rd, Read LUT Data Inc Add

#define cmdWrLUTInc         0x0C  // wr, Load LUT Data Inc Add

#define cmdRdCtrB           0x0E  // rd, Read Counter "B"

#define cmdLocReset         0x0E  // wr, Generate local reset

#define cmdLdCtrBIniReg     0x10  // wr, Load CTRB INITIAL Register

#define cmdGenTstClkB       0x12  // wr, Generate Test CLK B

#define cmdLdLUTCtr         0x14  // wr, Load LUT CTR (8 LSBs)

#define cmdLdLUTPgReg       0x16  // wr, Load LUT Page Register

#define cmdLdLUTDisPgReg    0x18  // wr, Load LUT Display Page
                                  // Register

                                  // (MSB's) D10, D9, D8

#define cmdClr0DegInt       0x1A // rd, Clear 0 Degree Interrupt

#define cmdLdParmReg        0x1A // wr, Load Parameter Register

                                  // D0 EN_CTR0_1

                                  // D1 EN_CTR2

                                  // D2 SYSTEM MASTER

                                  // D3 INT0_EN

                                  // D4 INT1_EN

                                  // D5 PG_INT_EN

#define cmdClr180DegInt     0x1C // rd, Clear 180 Degree Interrupt

#define cmdClrPageInt       0x1E // rd, Clear Page Interrupt

//

// 8-Bit I/O Commands

//
```

```
#define cmdCtr0Cs           0x20 // rd/wr, 82C54 CTR0 CS
#define cmdCtr1Cs           0x21 // rd/wr, 82C54 CTR1 CS
#define cmdCtr2Cs           0x22 // rd/wr, 82C54 CTR2 CS
#define cmdCtrCsCw          0x23 // rd/wr, 82C54 CW CS
#define cmdSelCtrBCtDwn     0x24 // rd/wr, Sel CTRB CT DOWN
#define cmdSelCtrBCtUp      0x25 // rd/wr, Sel CTRB CT UP
//
// 82C54 Ctr Commands
//
#define MODE2               0x4
#define RWBOTH              0x30
#define CTR0                0x0

//
// Param Reg Commands
//
#define EN_CTR0             0x0001
#define EN_CTR2             0x0002
#define SYS_MAS             0x0004
#define INT0_EN             0x0008
#define INT1_EN             0x0010
#define PGINT_EN            0x0020

//
// IO Rd/Wr Commands
//
#define IO8RD(CMD)        (inp(CMD))
#define IO8WR(CMD,VAL)    (outp(CMD, VAL))
#define IO16RD(CMD)       (inpw(CMD))
#define IO16WR(CMD,VAL)   (outpw(CMD, VAL))

#endif
```

The 3-D Volumetric #3 Control Card I/O Command Set

A September 1997, the 3-D Volumetric #3 Control Cards have not been fully debugged yet and, therefore, are not operational. However, many of the principles discussed here can be easily applied to the 3-D Volumetric #3 Control Cards. In fact, application software developed for the second-generation 3-D Volumetric Display System should be designed so that a low-end I/O command module unit utilizing the Volumetric #2 Command Set can be easily replaced with a module utilizing the Volumetric #3 Command Set.

The V3IO.H source header file is given below should the 3-D Volumetric #3 Control Cards become available in the near future.

```
//
// V3IO.H
//

#ifndef V3IOH
#define V3IOH

#include <dos.h>
#include <conio.h>

//
// 16-Bit I/O Commands
//
#define cmdRdMLReg           0x00  // rd, Read ML Register
#define cmdTstLdCtrB         0x00  // wr, Test Parallel LD CTRB
                                   // (Parallel Ld Contents of
                                   // Initial Register into CTRB
                                   // for Computer Test)
#define cmdRdXTbl            0x06 // rd, Rd X TBL
#define cmdWrXTbl            0x06 // wr, Ld X TBL
#define cmdRdYTbl            0x08 // rd, Rd Y TBL
#define cmdWrYTbl            0x08 // wr, Ld Y TBL
#define cmdLdSpdReg          0x0A // wr, Ld Motor Speed Register
#define cmdRdLUTInc          0x0C // rd, Rd LUT Data Inc ADD
#define cmdWrLUTInc          0x0C // wr, Ld LUT Data Inc ADD
```

```
#define cmdRdCtrB            0x0E // rd, Rd CTRB
#define cmdLocReset          0x0E // wr, LOC RESET (Local Reset)
#define cmdRdUpp16MemB       0x10 // rd, Rd Upper16 MemB Output
                                  // Register
#define cmdLdCtrBInitReg     0x10 // wr, Ld CTRB Initial Register
#define cmdRdLow16MemB       0x12 // rd, Rd Lower16 MemB Output
                                  // Register
#define cmdTstCtrB           0x12 // wr, Test CTRB
#define cmdRdLow16ShftRegClr 0x14 // rd, Rd Shaft Register Lower16
                                  // then CLR
#define cmdLdLUTCtr          0x14 // wr, Ld LUT CTR
#define cmdRdUpp16ShftRegClr 0x16 // rd, Rd Shaft Register Upper16
                                  //  then CLR
#define cmdLdLUTPgReg        0x16 // wr, Ld LUT PG Register
#define cmdRdParReg          0x18 // rd, Rd Parameter Register
#define cmdLdLUTDispPgReg    0x18 // wr, Ld LUT Display PG Register
#define cmdClr0degInt        0x1A // rd, CLR 0 Deg Int
#define cmdLdParamReg        0x1A // wr, Load Parameter Register
                                  // D0 - EN CTR0_1
                                  // D1 - EN CTR2
                                  // D2 - System Master
                                  // D3 - INT0 EN
                                  // D4 - INT1 EN
                                  // D5 - PG INT EN
                                  // D6 - X 16K Bank1
                                  // D7 - Y 16K Bank1
                                  // D8 - Enable 0 Index
                                  // D9 - Enable 180 Index
                                  // D10 - Half Rev Shaft CT
                                  // D11 - Spare
                                  // D12 - Ch_Sel_LSB
                                  // D13 - Ch_Sel_MSB
                                  // D14 - Select_Index_Rotation
```

```
                                // D15 - Spare
#define cmdClr180degInt      0x1C // rd, CLR 180 Deg Int
#define cmdClrPageInt        0x1E // rd, CLR Page Int

//
// 8-Bit I/O Commands
//
#define cmdCtr0Cs            0x20 // rd/wr, 82C54 CTR0 CS
#define cmdCtr1Cs            0x21 // rd/wr, 82C54 CTR1 CS
#define cmdCtr2Cs            0x22 // rd/wr, 82C54 CTR2 CS
#define cmdCtrCsCw           0x23 // rd/wr, 82C54 CW CS
#define cmdSelCtrBCtDwn      0x24 // rd/wr, Sel CTRB CT DWN
#define cmdSelCtrBCtUp       0x25 // rd/wr, Sel CTRB CT UP

//
// 82C54 Ctr Commands
//
#define MODE2                0x04
#define RWBOTH               0x30
#define CTR0                 0x00

//
// Param Reg Commands
//
#define EN_CTR0              0x0001
#define EN_CTR2              0x0002
#define SYS_MAS              0x0004
#define INT0_EN              0x0008
#define INT1_EN              0x0010
#define PGINT_EN             0x0020
#define X16KBNK1             0x0040
#define Y16KBNK1             0x0080
#define EN_0_INDX            0x0100
```

```
#define EN_180_INDX          0x0200
#define EN_HF_SHFT_CT        0x0400

//
// IO Rd/Wr Commands
//
#define IO8RD(CMD)          (inp(CMD))
#define IO8WR(CMD,VAL)      (outp(CMD, VAL))
#define IO16RD(CMD)         (inpw(CMD))
#define IO16WR(CMD,VAL)     (outpw(CMD, VAL))

#endif
```

APPENDIX 4-B. VIEW2DEVICE2MEMORY SOURCE LISTING

Below is the source listing for function VIEW2DEVICE2MEMORY, which is a defined member function for the VCC class (VCC.HPP and VCC.CPP). This function implements the algorithm discussed in section 4.8.

```
//
// GLOBAL VARIABLES FOR VIEW2DEVICE2MEMORY
//
float    xp, zp;
float    zp;
float    endpt1, endpt2;
float    ap1, bp1;
unsigned mem_offset;
float    theta;
VOXEL    mem_voxel;
unsigned *hibuf;

//
// VIEW2DEVICE2MEMORY
// (This is a poorly written function, I will have to optimize later)
//
void VCC::view2device2memory(float x, float y, float z,
          zGSList<unsigned> *buffer, short chnnl)
{
   // Do not render voxels in the dead center of the display ...
   if (sqrtf(x*x + z*z) <= DEAD_ZONE)
      return;

   // Calculate which quadrant voxel is in ... many ways to do this
   theta = atan2(x, -z);
   while (theta < 0)
      theta += TwoPi;
```

```
if (theta >= ThreePiDivTwo)
   chnnl = chA;
else if (theta >= Pi)
   chnnl = chB;
else if (theta >= PiDivTwo)
   chnnl = chC;
else if (theta >= 0.0)
   chnnl = chD;
else
   return;

// If TwoD mode is activated, then all images will be rendered on
// a single plane.
if (TwoD)
   y = sav_mid_disp_y;

// Figure out what cell to place voxel in ...
theta += (y * TwoPiDivYmax);
while (theta >= TwoPi)
   theta -= TwoPi;
mem_offset = (unsigned) ((max_voxels / 4.0) * (theta / Pi));
mem_offset *= 4;
mem_offset += chnnl;
if (mem_offset > MAXRAMCELL)
   return;

// Find the correlating x,z scan deflections based upon real
// world
// coords of the voxel ... In other words, map from real world
// coordinates to scanner deflection coordinates ... keep in mind
// that this is quadrant dependent.
switch (chnnl)
{
   case chA:
```

```
endpt1 = X1_chA + (X1off_chA * (y / max_disp_y));
endpt2 = X4_chA - (X4off_chA * (y / max_disp_y));
xp = (x - X4_chA) * ((endpt1 - endpt2) / (X1_chA - X4_chA))
        +endpt2;

endpt1 = Z3_chA + (Z3off_chA * (y / max_disp_y));
endpt2 = Z4_chA - (Z4off_chA * (y / max_disp_y));
zp = (z - Z4_chA) * ((endpt1 - endpt2) / (Z3_chA - Z4_chA))
        +endpt2;

ap1 = (xp - X1_chA) * ((B4_chA - B1_chA) / (X4_chA -
      X1_chA)) + B1_chA;
bp1 = (zp - Z3_chA) * ((A4_chA - A3_chA) / (Z4_chA -
      Z3_chA)) + A3_chA;
break;

case chB:
endpt1 = X1_chB + (X1off_chB * (y / max_disp_y));
endpt2 = X4_chB - (X4off_chB * (y / max_disp_y));
xp = (x - X4_chB) * ((endpt1 - endpt2) / (X1_chB - X4_chB))
        +endpt2;

endpt1 = Z3_chB + (Z3off_chB * (y / max_disp_y));
endpt2 = Z4_chB - (Z4off_chB * (y / max_disp_y));
zp = (z - Z4_chB) * ((endpt1 - endpt2) / (Z3_chB - Z4_chB))
        +endpt2;

ap1 = (xp - X1_chB) * ((B4_chB - B1_chB) / (X4_chB -
      X1_chB)) + B1_chB;
bp1 = (zp - Z3_chB) * ((A4_chB - A3_chB) / (Z4_chB -
      Z3_chB)) + A3_chB;
break;

case chC:
endpt1 = X1_chC + (X1off_chC * (y / max_disp_y));
endpt2 = X4_chC - (X4off_chC * (y / max_disp_y));
```

```
        xp = (x - X4_chC) * ((endpt1 - endpt2) / (X1_chC - X4_chC))
                +endpt2;

        endpt1 = Z3_chC + (Z3off_chC * (y / max_disp_y));
        endpt2 = Z4_chC - (Z4off_chC * (y / max_disp_y));
        zp = (z - Z4_chC) * ((endpt1 - endpt2) / (Z3_chC - Z4_chC))
                +endpt2;

        ap1 = (xp - X4_chC) * ((B1_chC - B4_chC) / (X1_chC -
              X4_chC)) + B4_chC;
        bp1 = (zp - Z3_chC) * ((A4_chC - A3_chC) / (Z4_chC -
              Z3_chC)) + A3_chC;
        break;

    case chD:
        endpt1 = X1_chD + (X1off_chD * (y / max_disp_y));
        endpt2 = X4_chD - (X4off_chD * (y / max_disp_y));
        xp = (x - X4_chD) * ((endpt1 - endpt2) / (X1_chD - X4_chD))
                + endpt2;

        endpt1 = Z3_chD + (Z3off_chD * (y / max_disp_y));
        endpt2 = Z4_chD - (Z4off_chD * (y / max_disp_y));
        zp = (z - Z4_chD) * ((endpt1 - endpt2) / (Z3_chD - Z4_chD))
                + endpt2;

        ap1 = (xp - X4_chD) * ((B1_chD - B4_chD) / (X1_chD -
              X4_chD)) + B4_chD;
        bp1 = (zp - Z3_chD) * ((A4_chD - A3_chD) / (Z4_chD -
              Z3_chD)) + A3_chD;
        break;
}

mem_voxel.vox.x = (unsigned) bp1;
mem_voxel.vox.y = (unsigned) ap1;
mem_voxel.vox.i = 255;

// Place voxel in memory cell ... If cell is occupied, find an
// appropriate neighbor cell to store it in ...
```

```
    register int i;
    register short found_empty_cell_flag = 0;
    register unsigned neighbor_memory_cell;

    if (*(ram_ptr + mem_offset))
    {
       neighbor_memory_cell = 0;
       for (i = 0; i < MAX_NEIGHBOR; i = (i > 0) ? -i : 1 - i)
       {
          neighbor_memory_cell = mem_offset + (i * 4);
          hibuf = ram_ptr + neighbor_memory_cell;
          if ((neighbor_memory_cell < MAXRAMCELL) &&
          (neighbor_memory_cell >= 0) &&  (*hibuf == 0))
          {
             found_empty_cell_flag = 1;
             break;
          }
       }
    }

    // The variable hibuf is our pointer to the 3-D Volumetric Display
    // Memory.
    if (!found_empty_cell_flag)
       hibuf = ram_ptr + mem_offset;

    *hibuf = mem_voxel.voxel;

    if (buffer)
       buffer->append(new unsigned((unsigned)hibuf));
}
```

APPENDIX 4-C. SOFTWARE DEFLECTION CALIBRATION INSTRUCTIONS FOR HELICAL 3-D VOLUMETRIC DISPLAY SYSTEMS

INTRODUCTION

The current helicoid-based 3-D volumetric display systems require calibration to align the four channels (quadrants) to achieve the following results:

a. Accurate rendering of images that span across multiple quadrants

b. Alignment of colors Red, Green, and Blue with one another to achieve color mixing and accurate rendering

The software-controlled calibration data are stored in individual files for each color. Red.cfg, Grn.cfg, and Blue.cfg are located in the same directory as the application. These files have three parts:

a. System hardware settings

b. Channel locations

c. Deflection offsets at the bottom of chamber

The Electronics section contains information about the orientation of each channel, the rotation speed of the helix, and values of various low-level registers used to control the system via the PC Control Card. These settings are not modified in calibration.

CHANNEL LOCATIONS

Each channel of a color has a different orientation due to changes in the setup of the optics (figure 4-A1). Before measurements are made, study the CFG file to find the correspondence between program variables and points on the display for each channel. A sample *.cfg file is provided as an example at the end of this chapter. Any line that begins with a '#' is a remark. The eight lines of each channel that are important now are X1_ch*, X2_ch*, X3_ch*, X4_ch*, Y1_ch*, Y2_ch*, Y3_ch*, and Y4_ch* (where * is whatever channel being aligned). To figure out where each point lies in the actual chamber, one must plot the points. For instance, in the supplied sample, the *.cfg file in CHANNEL A point, P1=(X1, Y1), has a 'small' value for X and large, positive value for Y. Thus, in channel A, P1 is located in the upper right corner (see coordinate axes). Remember that the coordinate axes are oriented as viewed from the front of the viewing chamber.

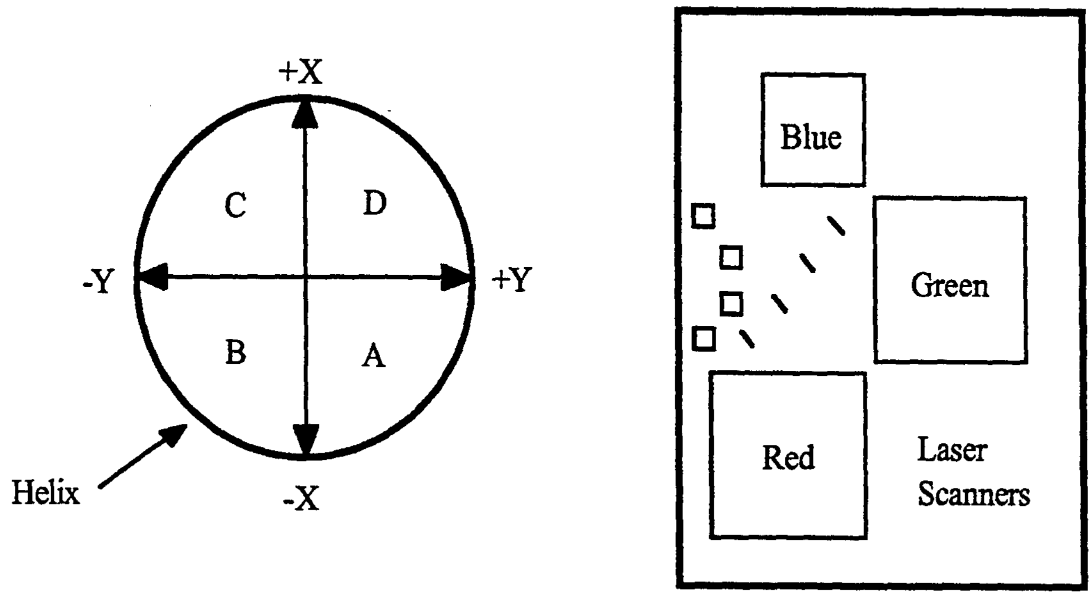

Figure 4-A1. Orientation of helix axes for calibration procedures.

After interpreting which variables in the *.cfg file correspond to which points in the display system, use the diagnostic menu program to input the five-line pattern. This creates vertical lines in the display at the center and each extreme corner of each channel. (Note: If the channels do not overlap slightly, as should be visible with the five-line pattern, then calibration will be impossible). The optics must be adjusted by a knowledgeable technician for these to overlap (see the section below on Optical Alignment). Now, use a ruler and some standard graph paper to measure and plot each of the corner points for each channel according to the coordinate system in figure 4-A2. All should be in inches, and all measurements should be written down as well as plotted because the next step is to enter each measurement into the *.cfg file.

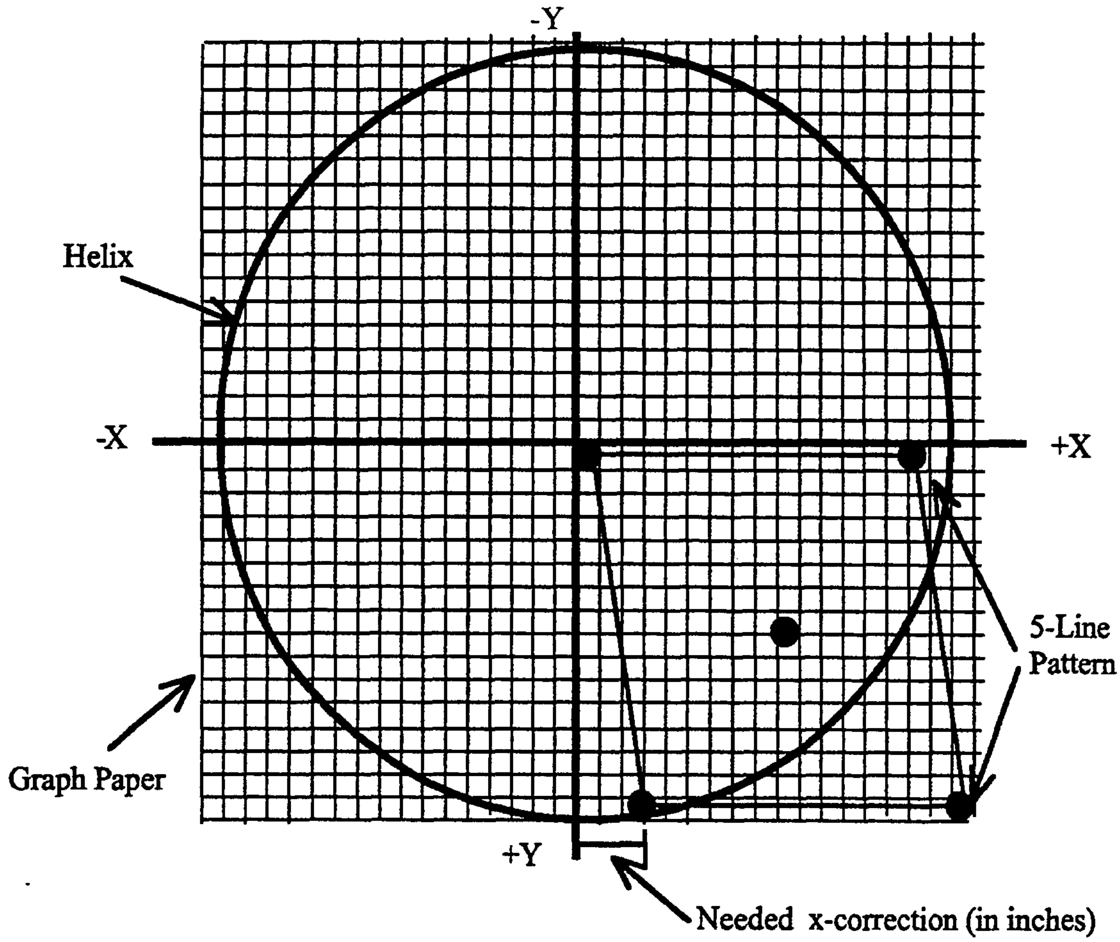

Figure 4-A2. Example of measuring the corner coordinates.

DEFLECTION OFFSETS

After 'dialing in' the locations of the channel extrema, the next step is to become familiar with a constantly evolving utility in the demonstration program. It is hidden item number 98 in the demonstration menu. When the item is selected, two submarines will come into view in the viewing chamber; one is red and the other green. The red submarine can be moved via the keyboard using the 'y', 'g', 'h', and 'b' keys, while the green is moved by the gray arrow keypad. Vertical movement for the green is achieved using 'z' and 'x', and will spin using the 'c' key. Both submarines can be moved to the same spot and then moved together simultaneously using the 'o', 'k', 'l', and ',' keys. They can be raised and lowered together using '[' and ']' and spun in both directions with 'C' and 'V'.

The free movement of these submarines enables viewing of how far off the alignment is from channel to channel, as well as from color to color. The ideal is to obtain a continuous picture without truncation from channel to channel at all heights and to have the colors align with one another so that color mixing can be achieved so that the images using both colors make sense. (For example, a red submarine shoots a green torpedo and hits the blue aircraft carrier.)

Use the following two steps to achieve further alignment of the channels:

1. Run the demonstration program, move the submarine to span across two channels, and note which channel should be moved which direction.

2. Go to the corresponding *.cfg file and 'fudge' the inputs of variables to move the channel closer into alignment.

To align channels closer to the bottom of the chamber, additional variables are used in the *.cfg file. These are the variables with names that contain the word 'off.' Each of these can be thought of as directly under the point, with the same name, but without 'off'. The changing of these variables will not affect the current calibration settings at the top of the chamber! They are used to "swing" the lower corners of each channel into alignment and then interpolation is used in the software to align the edges based on these points. The points cannot be seen unless the chamber is moving. The points are at the bottom of the chamber where the viewer cannot get inside. This makes it impossible to measure how far to swing these points.

Thus, the fine adjustments of the channels with one another and the coordination of the deflections truly ensure that CALIBRATION IS AN ART! There is no exact way to do it every time, because the optics involved can never all be in exactly the same position at the same time.

Red.cfg file
(Note: Z has replaced Y in this example)

NAME RED_VCC		
BASEADDR F40000	#	#
BASEIO 340	# CHANNEL D	# CHANNEL C
PARREG 3B	#	#
INITREG 0	H0_chD 0.0	H0_chC 0.0
REFRESH_PER_SEC 20.0	X0_chD 0.0	X0_chC 0.0
CTR0_VALUE 19	Z0_chD 0.0	Z0_chC 0.0
DISPLAYORI 0.0 0.0 0.0	X1_chD 0.0	X1_chC 0.0
DISPLAYSCALE 0.85 0.85 0.85	Z1_chD 18.0	Z1_chC 0.0
	X2_chD 0.0	X2_chC 0.0
DISPLAYOFFSET 0.0 0.0 0.0	Z2_chD 0.0	Z2_chC −18.0
	X3_chD −18.0	X3_chC −18.0
	Z3_chD 0.0	Z3_chC −18.0
	X4_chD −18.0	X4_chC −18.0
	Z4_chD 18.0	Z4_chC 0.0
	A1_chD 4095	A1_chC 4095
	B1_chD 4095	B1_chC 4095
	A2_chD 4095	A2_chC 4095
	B2_chD 0	B2_chC 0
	A3_chD 0	A3_chC 0
	B3_chD 0	B3_chC 0
	A4_chD 0	A4_chC 0
	B4_chD 4095	B4_chC 4095

#	#	APoff_chA 0
# CHANNEL B	# CHANNEL A	BPoff_chA 0
	#	
H0_chB 0.0	H0_chA 0.0	APoff_chB 0
X0_chB 0.0	X0_chA 0.0	BPoff_chB 0
Z0_chB 0.0	Z0_chA 0.0	
		APoff_chC 0
X1_chB 1.0	X1_chA 1.0	BPoff_chC 0
Z1_chB 0.0	Z1_chA 16.0	
X2_chB 1.0	X2_chA 1.0	APoff_chD 0
Z2_chB –15.5	Z2_chA 0.0	BPoff_chD 0
X3_chB 15.0	X3_chA 16.25	
Z3_chB –15.75	Z3_chA 0.0	X1off_chA 0.0
X4_chB 16.25	X4_chA 16.25	X4off_chA 0.0
Z4_chB 0.0	Z4_chA 15.75	Z3off_chA 0.0
		Z4off_chA 0.0
A1_chB 0	A1_chA 0	
B1_chB 4095	B1_chA 4095	X1off_chB –0.35
A2_chB 0	A2_chA 0	X4off_chB –0.4
B2_chB 0	B2_chA 0	Z3off_chB 0.0
A3_chB 4095	A3_chA 4095	Z4off_chB –0.25
B3_chB 0	B3_chA 0	
A4_chB 4095	A4_chA 4095	X1off_chC 0.0
B4_chB 4095	B4_chA 4095	X4off_chC 0.0
		Z3off_chC 0.0
		Z4off_chC 0.0
		X1off_chD 0.0
		X4off_chD 0.0
		Z3off_chD 0.0
		Z4off_chD 0.0

OPTICAL ALIGNMENT FOR SOFTWARE CALIBRATION

Before performing any software calibration procedures, the images projected by the laser scanners into the four quadrants of the helix must be brought into a consistent, known configuration. The goal is to maneuver the inside corners of each projected scan area to coincide with the central axis at the top of the helix. This is accomplished for both red and green scanners by using the five-line pattern in the Menu program and re-positioning the images by adjusting the mirror and beam combiner mounts in the projection optics.

Figure 4-A3 indicates the location of the various components in the projection optics assembly. A change in a particular green scanner image location is made by adjusting the x–y tilt controls of the respective final output mirror for that channel (1-inch square mirrors at the end of the table). Adjusting the x–y tilt controls of the respective dichroic beam combiner makes a change in a particular red scanner location. The order of adjustment is important. The green channels must be adjusted prior to the red channels. The inside corners of each green five-line pattern are individually brought in to coincide with the central metal shaft at the top of the helix rotor assembly. Once this is done for all four green channels, the tilt controls for the final output mirrors should not be moved again. The red channels are then aligned in a similar fashion using the beam combiners. Ideally, the projection optics should be allowed to "rest" for about a day to make sure that they are fully relaxed in their mounts and that there is no additional creeping of the images. Then, the software calibration routine can proceed.

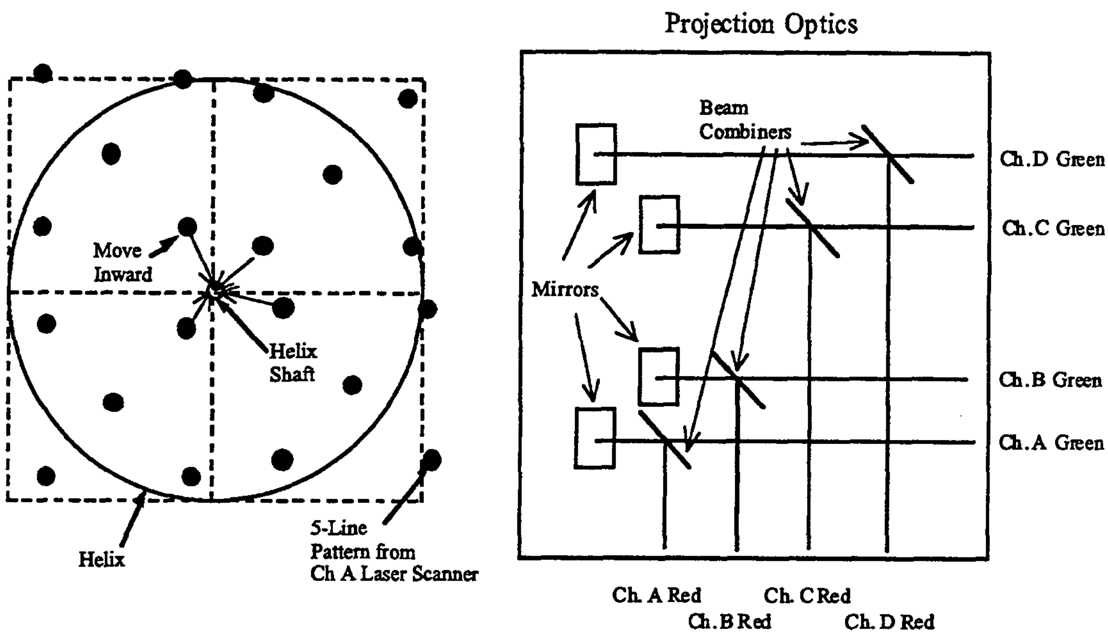

Figure 4-A3. Optical configuration for initial calibration.

SECTION 5. BIOGRAPHIES

PARVIZ SOLTAN

Parviz Soltan received his Bachelor of Science degree in Electrical Engineering from Lafayette College, his Master of Science degree in Physics from Syracuse University, and IE Engineering from Columbia University. He continued graduate studies and participated in the Ph.D. Program in Applied Physics at the University of California San Diego. He presently conducts research and development on flat-panel display technologies, fiber optics, and 3-D volumetric laser displays. He previously worked at IBM's Poughkeepsie and Kingston Laboratories on computer design and plasma display technology development. He has several patents and has published several technical papers. He is a former President of the Optical Society of San Diego.

MARK LASHER

Mark Lasher received his Bachelor of Science degree in Physics from the University of California San Diego in 1980. He received a Master of Science degree in physics from San Diego State University in 1983 and a Master of Science degree in electrical engineering from the University of California San Diego in 1989. He has been with Space and Naval Warfare Systems Center, San Diego, since 1983, working in acousto-optic laser scanning and integrated optic devices for microwave systems. His work has also included research in photorefractive materials, bistability, optical switching, A/D conversion, signal processing systems, and algorithm development. His most recent work is in the areas of laser scanners for display systems, laser colorimetry, and electro-optics.

WELDON DAHLKE

Weldon Dahlke received his Bachelor of Science degree in Electrical Engineering from the University of Colorado at Boulder, Colorado in 1961. Before coming to Naval Electronics Lab (NEL), he worked for Autonetics in Anaheim, CA as a Computer Field Engineer for the GAM 77 missile system at various Air Force and Navy installations. Since 1964, he has been with SSC San Diego and its predecessors Naval Command, Control and Ocean Surveillance Center RDT&E Division (NRaD), Naval Ocean Systems Center (NOSC) and NEL, working with experimental display techniques, technologies, and systems in the Command and Control arena. His specialty is designing, building, and testing digital and analog electronics for high-resolution video display systems. His latest design is a 10-layer electronic control board (containing 526 components) that fits into a standard PC and precisely controls the laser beam's position on the 3-D Double-Helix Display.

MALVYN MCDONALD

Malvyn McDonald received his Bachelor of Science and Master of Science degrees in Mechanical Engineering in 1971 and 1976 from San Diego State University. He has 23 years engineering experience with professional emphasis on design and development of shipboard, submarine, and shore-based communication systems, electronics and optics packaging systems, and structural and dynamic mechanical systems. He is experienced in development of systems, including testing, evaluation, and engineering documentation.

NEIL ACANTILADO

Neil Acantilado received a Bachelor of Science degree in Mathematics-Computer Science from the University of California San Diego. Early in his young career, he successfully worked as a software

engineer at the following companies: Foodmaker Inc., Zybex Inc., SDSU Foundation (a student contracting agency for SSC San Diego), and Horizons Technology Inc. However, it was as a student contractor that he was first able to participate in the software development of the 3-D Laser-Based Volumetric Display System. As a result, he has created system device drivers, diagnostic software, and image-rendering algorithms for the 3-D Volumetric Display. He has also developed application software that demonstrates the the real-time capabilities of the 3-D Volumetric Display. An example includes a real-time 3-D air traffic control application. It is important to note that a U.S. patent has been applied for this application. He was hired as a New Professional at NRaD (now SSC San Diego) in 1995.

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The Space and Naval Warfare (SPAWAR) Systems Center, San Diego (SSC San Diego) Simulation and Human Technology Division has developed and improved its second-generation 3-D Volumetric Display System for displaying data, information, and scenes in a three-dimensional volume of image space. The system has good potential for many military and commercial applications. Based on a computer-controlled laser optics system that projects three laser beams simultaneously onto a 36-inch diameter/18-inch-high double helix spinning at 600 revolutions per minute, this system presents 3-D images in an addressable 10 cubic feet of cylindrical volume. This report discusses the four basic disciplines used in development of the Improved Second-Generation 3-D Volumetric Display System and provides examples of practical applications of the technology.

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